

## 16-BIT SINGLE-CHIP MICROCONTROLLER

**DESCRIPTION**

The  $\mu$ PD78P4908, 78K/IV series' product, is a one-time PROM version of the  $\mu$ PD784907 and  $\mu$ PD784908 with internal mask ROM.

Since user programs can be written to PROM, this microcomputer is best suited for evaluation in system development, manufacture of small quantities of multiple products, and fast start-up of applications.

**For specific functions and other detailed information, consult the following user's manuals.**

**These manuals are required reading for design work.**

$\mu$ PD784908 Subseries User's Manual - Hardware : U11787E

78K/IV Series User's Manual - Instruction : U10905E

**FEATURES**

- 78K/IV series
- Internal PROM: 128 Kbytes
- Internal RAM: 4,352 bytes
- ★ • Supply voltage:  $V_{DD} = 4.5$  to  $5.5$  V  
(At main clock:  $f_{xx} = 12.58$  MHz, internal system clock =  $f_{xx}$ :  $f_{CYK} = 79$  ns)  
 $V_{DD} = 4.0$  to  $5.5$  V  
(Other than above:  $f_{CYK} = 159$  ns)

**ORDERING INFORMATION**

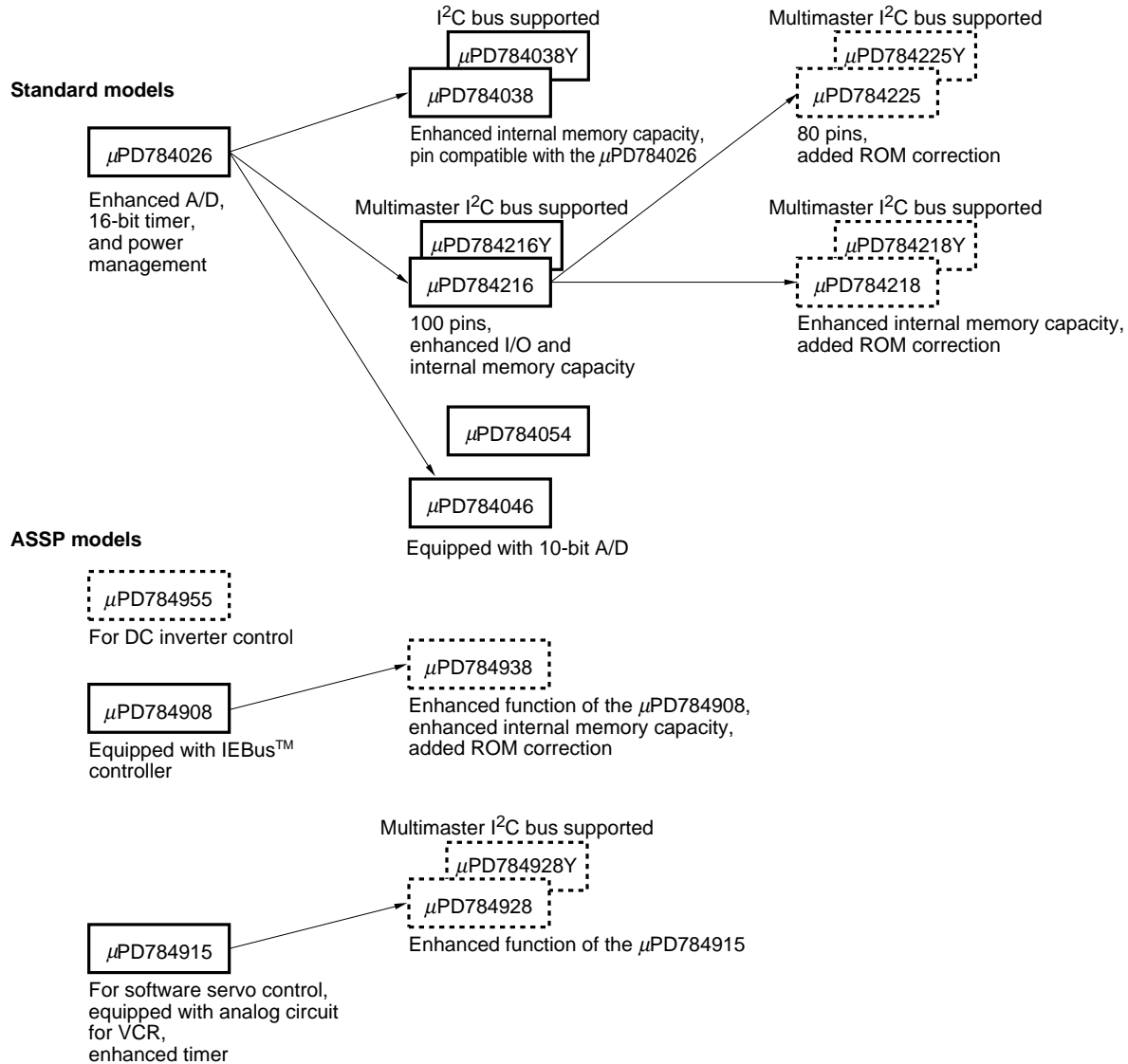
Part number	Package	Internal ROM
$\mu$ PD78P4908GF-3BA	100-pin plastic QFP (14 × 20 mm)	One-time PROM

The information in this document is subject to change without notice.

★ 78K/IV SERIES PRODUCT DEVELOPMENT DIAGRAM

: Under mass production

: Under development



FUNCTIONS

(1/2)

Item		Function	
Number of basic instructions (mnemonics)		113	
General-purpose register		8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)	
★	Minimum instruction execution time	<ul style="list-style-type: none"> <li>• 320 ns/636 ns/1.27 μs/2.54 μs (at 6.29 MHz)</li> <li>• 160 ns/320 ns/636 ns/1.27 μs (at 12.58 MHz)</li> </ul>	
Internal memory	ROM	128 Kbytes	
	RAM	4,352 bytes	
Memory space		Program and data: 1 Mbyte	
I/O ports	Total	80	
	Input	8	
	Input/output	72	
Additional function pins <sup>Note</sup>	LED direct drive outputs	24	
	Transistor direct drive	8	
	N-ch open drain	4	
Real-time output ports		4 bits × 2, or 8 bits × 1	
IEBus controller		Incorporated (simple version)	
Timer/counter	Timer/counter 0: (16 bits)	Timer register × 1 Capture register × 1 Compare register × 2	Pulse output capability <ul style="list-style-type: none"> <li>• Toggle output</li> <li>• PWM/PPG output</li> <li>• One-shot pulse output</li> </ul>
	Timer/counter 1: (16 bits)	Timer register × 1 Capture register × 1 Capture/compare register × 1 Compare register × 1	Real-time output port
	Timer/counter 2: (16 bits)	Timer register × 1 Capture register × 1 Capture/compare register × 1 Compare register × 1	Pulse output capability <ul style="list-style-type: none"> <li>• Toggle output</li> <li>• PWM/PPG output</li> </ul>
	Timer 3: (16 bits)	Timer register × 1 Compare register × 1	
★	Clock timer	Interrupt requests are generated at 0.5-second intervals. (A clock timer oscillator is incorporated.) Either the main clock (6.29 MHz/12.58 MHz) or real-time clock (32.768 kHz) can be selected as the input clock.	
Clock output		Selected from f <sub>CLK</sub> , f <sub>CLK</sub> /2, f <sub>CLK</sub> /4, f <sub>CLK</sub> /8, or f <sub>CLK</sub> /16 (can be used as a 1-bit output port)	
PWM outputs		12-bit resolution × 2 channels	
Serial interface		UART/IOE (3-wire serial I/O) : 2 channels (incorporating baud rate generator) CSI (3-wire serial I/O) : 2 channels	

**Note** Additional function pins are included in the I/O pins.

(2/2)

Item		Function
A/D converter		8-bit resolution × 8 channels
Watchdog timer		1 channel
Standby		HALT/STOP/IDLE mode
Interrupt	Hardware source	27 (20 internal, 7 external (sampling clock variable input: 1))
	Software source	BRK or BRKCS instruction, operand error
	Nonmaskable	1 internal, 1 external
	Maskable	19 internal, 6 external
		<ul style="list-style-type: none"> <li>• 4-level programmable priority</li> <li>• 3 operation statuses: vectored interrupt, macro service, context switching</li> </ul>
★ Power supply voltage		<ul style="list-style-type: none"> <li>• <math>V_{DD} = 4.5</math> to <math>5.5</math> V (At main clock: <math>f_{XX} = 12.58</math> MHz, internal system clock = <math>f_{XX}</math>: <math>f_{CYK} = 79</math> ns)</li> <li>• <math>V_{DD} = 4.0</math> to <math>5.5</math> V (Other than above: <math>f_{CYK} = 159</math> ns)</li> </ul>
Package		100-pin plastic QFP (14 × 20 mm)

## CONTENTS

1.	DIFFERENCES BETWEEN $\mu$ PD78P4908 AND MASK ROM PRODUCTS .....	6
2.	PIN CONFIGURATION (TOP VIEW) .....	7
3.	BLOCK DIAGRAM .....	10
4.	PIN FUNCTIONS .....	11
4.1	PINS FOR NORMAL OPERATING MODE .....	11
4.2	PINS FOR PROM PROGRAMMING MODE ( $V_{PP} \geq +5 \text{ V}$ or $+12.5 \text{ V}$ , $\overline{\text{RESET}} = \text{L}$ ) .....	14
4.2.1	Pin Functions .....	14
4.2.2	Pin Functions .....	15
4.3	I/O CIRCUITS FOR PINS AND HANDLING OF UNUSED PINS .....	16
5.	INTERNAL MEMORY SIZE SELECT REGISTER (IMS) .....	19
6.	PROM PROGRAMMING .....	20
6.1	OPERATION MODE .....	20
6.2	PROM WRITE SEQUENCE .....	22
6.3	PROM READ SEQUENCE .....	26
7.	SCREENING ONE-TIME PROM PRODUCTS .....	26
8.	ELECTRICAL CHARACTERISTICS .....	27
9.	PACKAGE DRAWING .....	51
10.	RECOMMENDED SOLDERING CONDITIONS .....	52
	APPENDIX A DEVELOPMENT TOOLS .....	53
	APPENDIX B CONVERSION SOCKET (EV-9200GF-100) PACKAGE DRAWING .....	56
	APPENDIX C RELATED DOCUMENTS .....	58

1. DIFFERENCES BETWEEN μPD78P4908 AND MASK ROM PRODUCTS

The μPD78P4908 is produced by replacing the mask ROM in the μPD784907 or μPD784908 with PROM to which data can be written. The functions of the μPD78P4908 are the same as those of the μPD784907 or μPD784908 except for the PROM specification such as writing and verification, except that the PROM size can be changed to 96 or 128 Kbytes, and except that the internal RAM size can be changed to 3,584 or 4,352 bytes.

Table 1-1 shows the differences between these products.

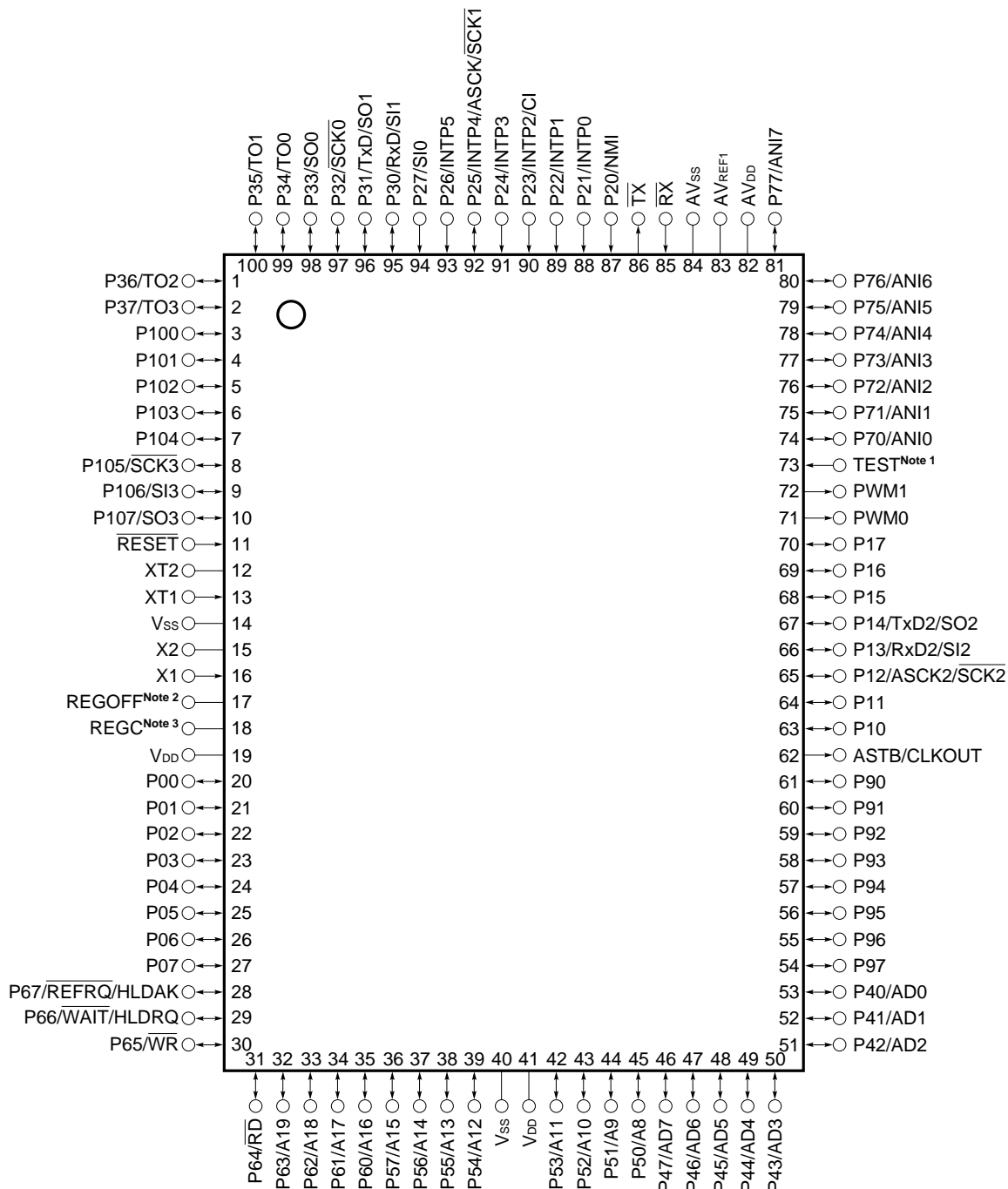
Table 1-1. Differences Between the μPD78P4908 and Mask ROM Products

Product name Item	μPD78P4908	μPD784907	μPD784908
Internal program memory	<ul style="list-style-type: none"> <li>• 128-Kbyte PROM</li> <li>• Can be changed to 96 Kbytes by IMS</li> </ul>	<ul style="list-style-type: none"> <li>• 96-Kbyte mask ROM</li> </ul>	<ul style="list-style-type: none"> <li>• 128-Kbyte mask ROM</li> </ul>
Internal RAM	<ul style="list-style-type: none"> <li>• 4,352-byte internal RAM</li> <li>• Can be changed to 3,584 bytes by IMS</li> </ul>	<ul style="list-style-type: none"> <li>• 3,584-byte internal RAM</li> </ul>	<ul style="list-style-type: none"> <li>• 4,352-byte internal RAM</li> </ul>
Pin connection	Pin functions related to writing or reading of PROM have been added to the μPD78P4908.		
★ Power supply voltage	<ul style="list-style-type: none"> <li>• V<sub>DD</sub> = 4.5 to 5.5 V (At main clock: f<sub>xx</sub> = 12.58 MHz, internal system clock = f<sub>xx</sub>: f<sub>CYK</sub> = 79 ns</li> <li>• V<sub>DD</sub> = 4.0 to 5.5 V (Other than above: f<sub>CYK</sub> = 159 ns)</li> </ul>	<ul style="list-style-type: none"> <li>• V<sub>DD</sub> = 4.0 to 5.5 V (At main clock: f<sub>xx</sub> = 12.58 MHz, internal system clock = f<sub>xx</sub>: f<sub>CYK</sub> = 79 ns)</li> <li>• V<sub>DD</sub> = 3.5 to 5.5 V (Other than above: f<sub>CYK</sub> = 159 ns)</li> </ul>	
Electrical characteristics	Partially differs between these products.		

2. PIN CONFIGURATION (TOP VIEW)

(1) Normal operation mode

- 100-pin plastic QFP (14 × 20 mm)  
μPD78P4908GF-3BA



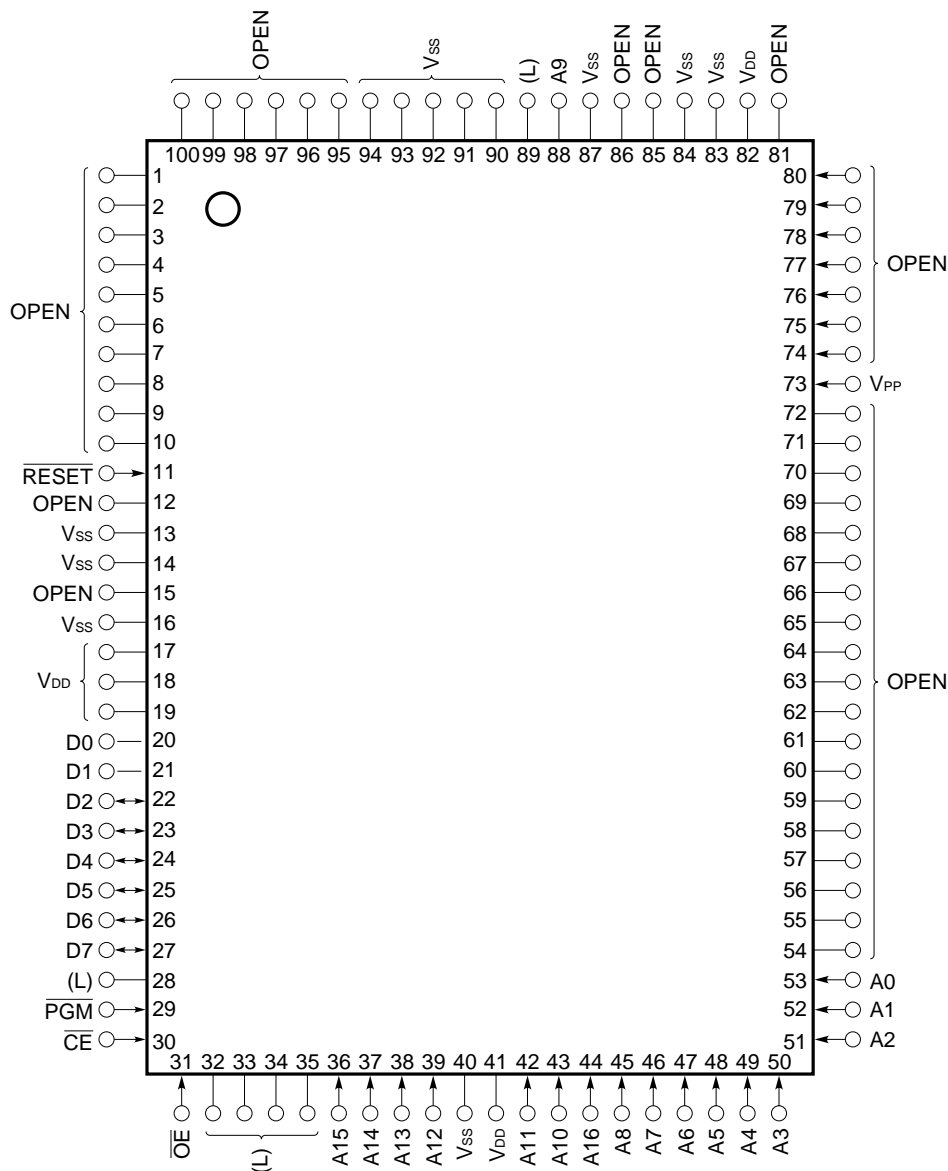
- Notes 1.** Connect the TEST pin to Vss directly.
2. Connect the REGOFF pin to Vss directly (select regulator operation)
  3. Connect the REGC pin to Vss through a 1-μF capacitor.

A8-A19	: Address bus	PWM0, PWM1	: Pulse width modulation output
AD0-AD7	: Address/data bus	$\overline{RD}$	: Read strobe
ANI0-ANI7	: Analog input	$\overline{REFRQ}$	: Refresh request
ASCK, ASCK2	: Asynchronous serial clock	REGC	: Regulator capacitance
ASTB	: Address strobe	REGOFF	: Regulator off
AV <sub>DD</sub>	: Analog power supply	$\overline{RESET}$	: Reset
AV <sub>REF1</sub>	: Reference voltage	$\overline{RX}$	: IEBus receive data
AV <sub>SS</sub>	: Analog ground	RxD, RxD2	: Receive data
CI	: Clock input	$\overline{SCK0-SCK3}$	: Serial clock
CLKOUT	: Clock output	SI0-SI3	: Serial input
HLD <sub>AK</sub>	: Hold acknowledge	SO0-SO3	: Serial output
HLD <sub>RQ</sub>	: Hold request	TEST	: Test
INTP0-INTP5	: Interrupt from peripherals	TO0-TO3	: Timer output
NMI	: Non-maskable interrupt	$\overline{TX}$	: IEBus transmit data
P00-P07	: Port 0	TxD, TxD2	: Transmit data
P10-P17	: Port 1	V <sub>DD</sub>	: Power supply
P20-P27	: Port 2	V <sub>SS</sub>	: Ground
P30-P37	: Port 3	$\overline{WAIT}$	: Wait
P40-P47	: Port 4	$\overline{WR}$	: Write strobe
P50-P57	: Port 5	X1, X2	: Crystal (main system clock)
P60-P67	: Port 6	XT1, XT2	: Crystal (watch)
P70-P77	: Port 7		
P90-P97	: Port 9		
P100-P107	: Port 10		



(2) PROM programming mode

- 100-pin plastic QFP (14 × 20 mm)  
μPD78P4908GF-3BA



**Caution L** : Connect these pins separately to the Vss pins through 10-kΩ pull-down resistors.

**Vss** : To be connected to the ground.

**Open** : Nothing should be connected on these pins.

**RESET**: Set a low-level input.

A0-A16 : Address bus

CE : Chip enable

D0-D7 : Data bus

OE : Output enable

PGM : Program

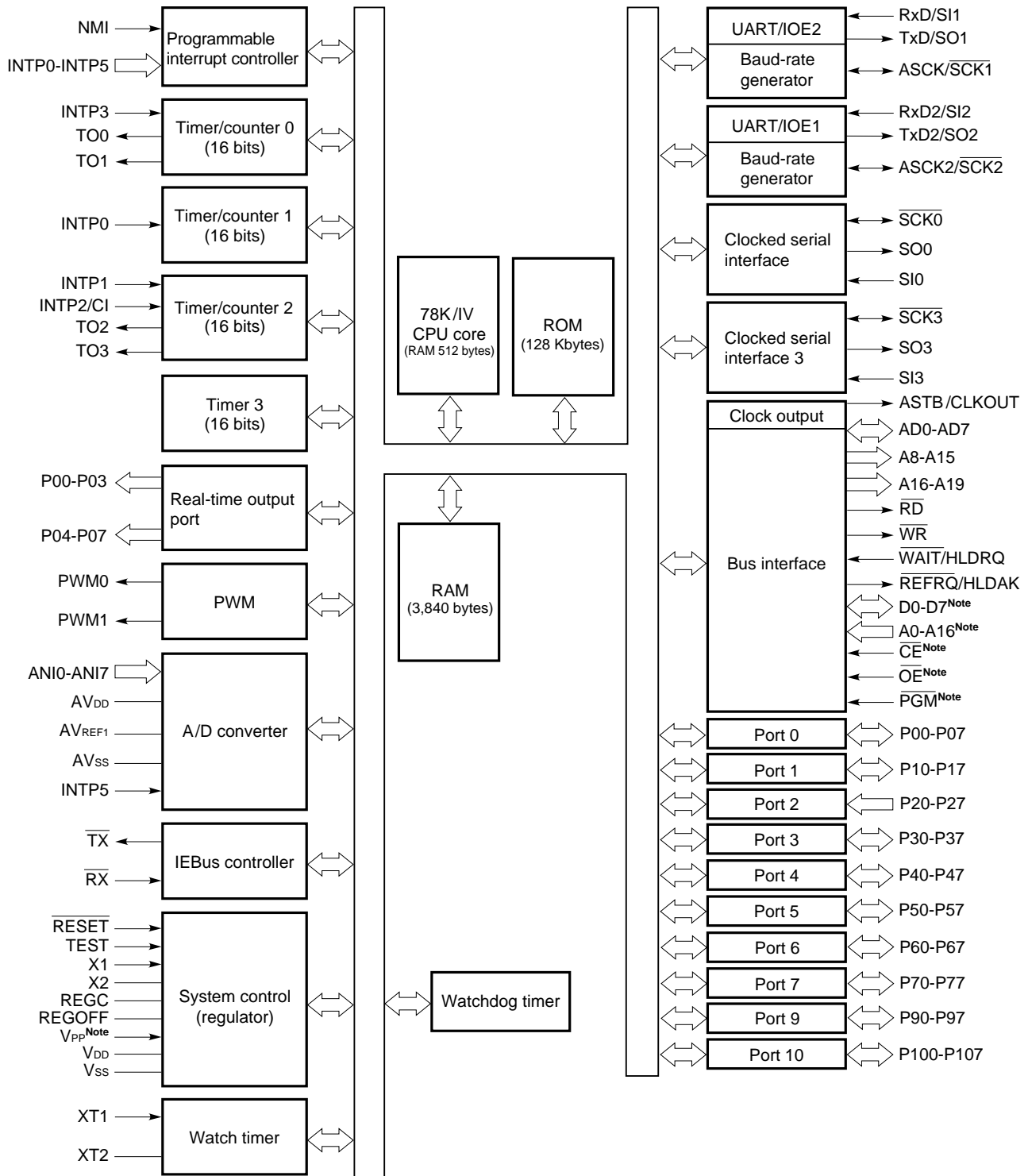
RESET : Reset

VDD : Power supply

VPP : Programming power supply

Vss : Ground

3. BLOCK DIAGRAM



**Note** In the PROM programming mode.

## 4. PIN FUNCTIONS

### 4.1 PINS FOR NORMAL OPERATING MODE

#### (1) Port pins (1/2)

Pin	I/O	Also used as	Function
P00-P07	I/O	—	Port 0 (P0): <ul style="list-style-type: none"> <li>• 8-bit I/O port.</li> <li>• Functions as a real-time output port (4 bits × 2).</li> <li>• Inputs and outputs can be specified bit by bit.</li> <li>• The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode.</li> <li>• Can drive a transistor.</li> </ul>
P10	I/O	—	Port 1 (P1): <ul style="list-style-type: none"> <li>• 8-bit I/O port.</li> <li>• Inputs and outputs can be specified bit by bit.</li> <li>• The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode.</li> <li>• Can drive LED.</li> </ul>
P11		—	
P12		ASCK2/ $\overline{\text{SCK2}}$	
P13		RxD2/SI2	
P14		TxD2/SO2	
P15-P17		—	
P20	Input	NMI	Port 2 (P2): <ul style="list-style-type: none"> <li>• 8-bit input-only port.</li> <li>• P20 does not function as a general-purpose port (nonmaskable interrupt). However, the input level can be checked by an interrupt service routine.</li> <li>• The use of built-in pull-up resistors can be specified by software for pins P22 to P27 (in units of 6 bits).</li> <li>• The P25/INTP4/ASCK/<math>\overline{\text{SCK1}}</math> pin functions as the <math>\overline{\text{SCK1}}</math> input/output pin by CSIM1.</li> </ul>
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP4/ASCK/ $\overline{\text{SCK1}}$	
P26		INTP5	
P27		SI0	
P30	I/O	RxD/SI1	Port 3 (P3): <ul style="list-style-type: none"> <li>• 8-bit I/O port.</li> <li>• Inputs and outputs can be specified bit by bit.</li> <li>• The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode.</li> <li>• P32 and P33 can be set as the N-ch open-drain pin.</li> </ul>
P31		TxD/SO1	
P32		$\overline{\text{SCK0}}$	
P33		SO0	
P34-P37		TO0-TO3	
P40-P47	I/O	AD0-AD7	Port 4 (P4): <ul style="list-style-type: none"> <li>• 8-bit I/O port.</li> <li>• Inputs and outputs can be specified bit by bit.</li> <li>• The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode.</li> <li>• Can drive LED.</li> </ul>

(1) Port pins (2/2)

Pin	I/O	Also used as	Function
P50-P57	I/O	A8-A15	Port 5 (P5): <ul style="list-style-type: none"> <li>• 8-bit I/O port.</li> <li>• Inputs and outputs can be specified bit by bit.</li> <li>• The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode.</li> <li>• Can drive LED.</li> </ul>
P60-P63	I/O	A16-A19	Port 6 (P6): <ul style="list-style-type: none"> <li>• 8-bit I/O port.</li> <li>• Inputs and outputs can be specified bit by bit.</li> <li>• The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode.</li> </ul>
P64		$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT/HLDRQ}$	
P67		$\overline{REFRQ/HLDAK}$	
P70-P77	I/O	ANI0-ANI7	Port 7 (P7): <ul style="list-style-type: none"> <li>• 8-bit I/O port.</li> <li>• Inputs and outputs can be specified bit by bit.</li> </ul>
P90-P97	I/O	—	Port 9 (P9): <ul style="list-style-type: none"> <li>• 8-bit I/O port.</li> <li>• Inputs and outputs can be specified bit by bit.</li> <li>• The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode.</li> </ul>
P100-P104	I/O	—	Port 10 (P10): <ul style="list-style-type: none"> <li>• 8-bit I/O port.</li> <li>• Inputs and outputs can be specified bit by bit.</li> <li>• The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode.</li> <li>• P105 and P107 can be set as the N-ch open-drain pin.</li> </ul>
P105		$\overline{SCK3}$	
P106		SI3	
P107		SO3	

(2) Non-port pins (1/2)

Pin	I/O	Also used as	Function
TO0-TO3	Output	P34-P37	Timer output
CI	Input	P23/INTP2	Input of a count clock for timer/counter 2
RxD	Input	P30/SI1	Serial data input (UART0)
RxD2		P13/SI2	Serial data input (UART2)
TxD	Output	P31/SO1	Serial data output (UART0)
TxD2		P14/SO2	Serial data output (UART2)
ASCK	Input	P25/INTP4/ $\overline{\text{SCK1}}$	Baud rate clock input (UART0)
ASCK2		P12/ $\overline{\text{SCK2}}$	Baud rate clock input (UART2)
SI0	Input	P27	Serial data input (3-wire serial I/O 0)
SI1		P30/RxD	Serial data input (3-wire serial I/O 1)
SI2		P13/RxD2	Serial data input (3-wire serial I/O 2)
SI3		P106	Serial data input (3-wire serial I/O 3)
SO0	Output	P33	Serial data output (3-wire serial I/O 0)
SO1		P31/TxD	Serial data output (3-wire serial I/O 1)
SO2		P14/TxD2	Serial data output (3-wire serial I/O 2)
SO3		P107	Serial data output (3-wire serial I/O 3)
$\overline{\text{SCK0}}$	I/O	P32	Serial clock I/O (3-wire serial I/O 0)
$\overline{\text{SCK1}}$		P25/INTP4/ASCK	Serial clock I/O (3-wire serial I/O 1)
$\overline{\text{SCK2}}$		P12/ASCK2	Serial clock I/O (3-wire serial I/O 2)
$\overline{\text{SCK3}}$		P105	Serial clock I/O (3-wire serial I/O 3)
NMI	Input	P20	External interrupt request
INTP0		P21	<ul style="list-style-type: none"> <li>Input of a count clock for timer/counter 1</li> <li>Capture/trigger signal for CR11 or CR12</li> </ul>
INTP1		P22	<ul style="list-style-type: none"> <li>Input of a count clock for timer/counter 2</li> <li>Capture/trigger signal for CR22</li> </ul>
INTP2		P23/CI	<ul style="list-style-type: none"> <li>Input of a count clock for timer/counter 2</li> <li>Capture/trigger signal for CR21</li> </ul>
INTP3		P24	<ul style="list-style-type: none"> <li>Input of a count clock for timer/counter 0</li> <li>Capture/trigger signal for CR02</li> </ul>
INTP4		P25/ASCK/ $\overline{\text{SCK1}}$	—
INTP5		P26	Input of a conversion start trigger for A/D converter
AD0-AD7	I/O	P40-P47	Time multiplexing address/data bus (for connecting external memory)
A8-A15	Output	P50-P57	High-order address bus (for connecting external memory)
A16-A19	Output	P60-P63	High-order address during address expansion (for connecting external memory)
$\overline{\text{RD}}$	Output	P64	Strobe signal output for reading the contents of external memory
$\overline{\text{WR}}$	Output	P65	Strobe signal output for writing on external memory
$\overline{\text{WAIT}}$	Input	P66/HLDRQ	Wait signal insertion
$\overline{\text{REFRQ}}$	Output	P67/HLDAK	Refresh pulse output to external pseudo static memory
HLDRQ	Input	P66/ $\overline{\text{WAIT}}$	Input of bus hold request
HLDAK	Output	P67/ $\overline{\text{REFRQ}}$	Output of bus hold response
ASTB	Output	CLKOUT	Latch timing output of time multiplexing address (A0-A7) (for connecting external memory)

(2) Non-port pins (2/2)

Pin	I/O	Also used as	Function
CLKOUT	Output	ASTB	Clock output
PWM0	Output	—	PWM output 0
PWM1	Output	—	PWM output 1
R $\bar{X}$	Input	—	Data input (IEBus)
T $\bar{X}$	Output	—	Data output (IEBus)
★ REGC	—	—	Capacitor connection for stabilizing the regulator output/Power supply when the regulator is stopped. Connect to V <sub>SS</sub> via a 1-μF capacitor.
★ REGOFF	—	—	Signal for specifying regulator operation. Directly connect to V <sub>SS</sub> (regulator selected).
$\overline{\text{RESET}}$	Input	—	Chip reset
X1	Input	—	Crystal input for system clock oscillation (A clock pulse can also be input to the X1 pin.)
X2	—		
XT1	Input	—	Real-time clock connection
XT2	—	—	
ANI0-ANI7	Input	P70-P77	Analog voltage inputs for the A/D converter
AV <sub>REF1</sub>	—	—	Application of A/D converter reference voltage
AV <sub>DD</sub>			Positive power supply for the A/D converter
AV <sub>SS</sub>			Ground for the A/D converter
V <sub>DD</sub>			Positive power supply
V <sub>SS</sub>			Ground
TEST			Input

4.2 PINS FOR PROM PROGRAMMING MODE (V<sub>PP</sub> ≥ +5 V or +12.5 V,  $\overline{\text{RESET}} = \text{L}$ )

4.2.1 Pin Functions

Pin name	I/O	Function
V <sub>PP</sub>	—	PROM programming mode selection High voltage input during program write or verification
$\overline{\text{RESET}}$	Input	PROM programming mode selection
A0-A16		Address bus
D0-D7	I/O	Data bus
$\overline{\text{CE}}$	Input	PROM enable input/program pulse input
$\overline{\text{OE}}$		Read strobe input to PROM
$\overline{\text{PGM}}$		Program/program inhibit input during PROM programming mode
V <sub>DD</sub>	—	Positive power supply
V <sub>SS</sub>	—	GND

#### 4.2.2 Pin Functions

**(1)  $V_{PP}$  (Programming power supply): Input**

Input pin for setting the  $\mu$ PD78P4908 to the PROM programming mode. When the input voltage on this pin is +6.5 V or more and when  $\overline{\text{RESET}}$  input goes low, the  $\mu$ PD78P4908 enters the PROM programming mode. When  $\overline{\text{CE}}$  is made low for  $V_{PP} = +12.5$  V and  $\overline{\text{OE}} = \text{high}$ , program data on D0 to D7 can be written into the internal PROM cell selected by A0 to A16.

**(2)  $\overline{\text{RESET}}$  (Reset): Input**

Input pin for setting the  $\mu$ PD78P4908 to the PROM programming mode. When input on this pin is low, and when the input voltage on the  $V_{PP}$  pin goes +5 V or more, the  $\mu$ PD78P4908 enters the PROM programming mode.

**(3) A0 to A16 (Address bus): Input**

Address bus that selects an internal PROM address (0000H to 1FFFFH)

**(4) D0 to D7 (Data bus): I/O**

Data bus through which a program is written on or read from internal PROM

**(5)  $\overline{\text{CE}}$  (Chip enable): Input**

This pin inputs the enable signal from internal PROM. When this signal is active, a program can be written or read.

**(6)  $\overline{\text{OE}}$  (Output enable): Input**

This pin inputs the read strobe signal to internal PROM. When this signal is made active for  $\overline{\text{CE}} = \text{low}$ , a one-byte program in the internal PROM cell selected by A0 to A16 can be read onto D0 to D7.

**(7)  $\overline{\text{PGM}}$  (Program): Input**

The input pin for the operation mode control signal of the internal PROM.

Upon activation, writing to the internal PROM is enabled.

Upon inactivation, reading from the internal PROM is enabled.

**(8)  $V_{DD}$**

Positive power supply pin

**(9)  $V_{SS}$**

Ground potential pin

4.3 I/O CIRCUITS FOR PINS AND HANDLING OF UNUSED PINS

Table 4-1 describes the types of I/O circuits for pins and the handling of unused pins.

Figure 4-1 shows the configuration of these various types of I/O circuits.

Table 4-1. Types of I/O Circuits for Pins and Handling of Unused Pins (1/2)

Pin	I/O circuit type	I/O	Recommended connection method for unused pins			
P00-P07	5-A	I/O	Input state: To be connected to V <sub>DD</sub> Output state: To be left open			
P10, P11						
P12/ASCK2/SCK2						
P13/RxD2/SI2						
P14/TxD2/SO2						
P15-P17						
P20/NMI	2	Input	To be connected to V <sub>DD</sub> or V <sub>SS</sub>			
P21/INTP0						
P22/INTP1	2-A			To be connected to V <sub>DD</sub>		
P23/INTP2/CI						
P24/INTP3						
P25/INTP4/ASCK/SCK1	8-A	I/O	Input state: To be connected to V <sub>DD</sub> Output state: To be left open			
P26/INTP5	2-A	Input	To be connected to V <sub>DD</sub>			
P27/SI0						
P30/RxD/SI1	5-A	I/O	Input state: To be connected to V <sub>DD</sub> Output state: To be left open			
P31/TxD/SO1						
P32/SCK0	10-A					
P33/SO0						
P34/TO0-P37/TO3	5-A					
P40/AD0-P47/AD7						
P50/A8-P57/A15						
P60/A16-P63/A19						
P64/RD						
P65/WR						
P66/WAIT/HLDRQ						
P67/REFRQ/HLDAK						
P70/ANI0-P77/ANI7				20	I/O	Input state: To be connected to V <sub>DD</sub> or V <sub>SS</sub> Output state: To be left open
P90-P97						
P100-P104	5-A					
P105/SCK3		10-A				
P106/SI3						
P107/SO3	10-A					
ASTB/CLKOUT	4	Output	To be left open			



Table 4-1. Types of I/O Circuits for Pins and Handling of Unused Pins (2/2)

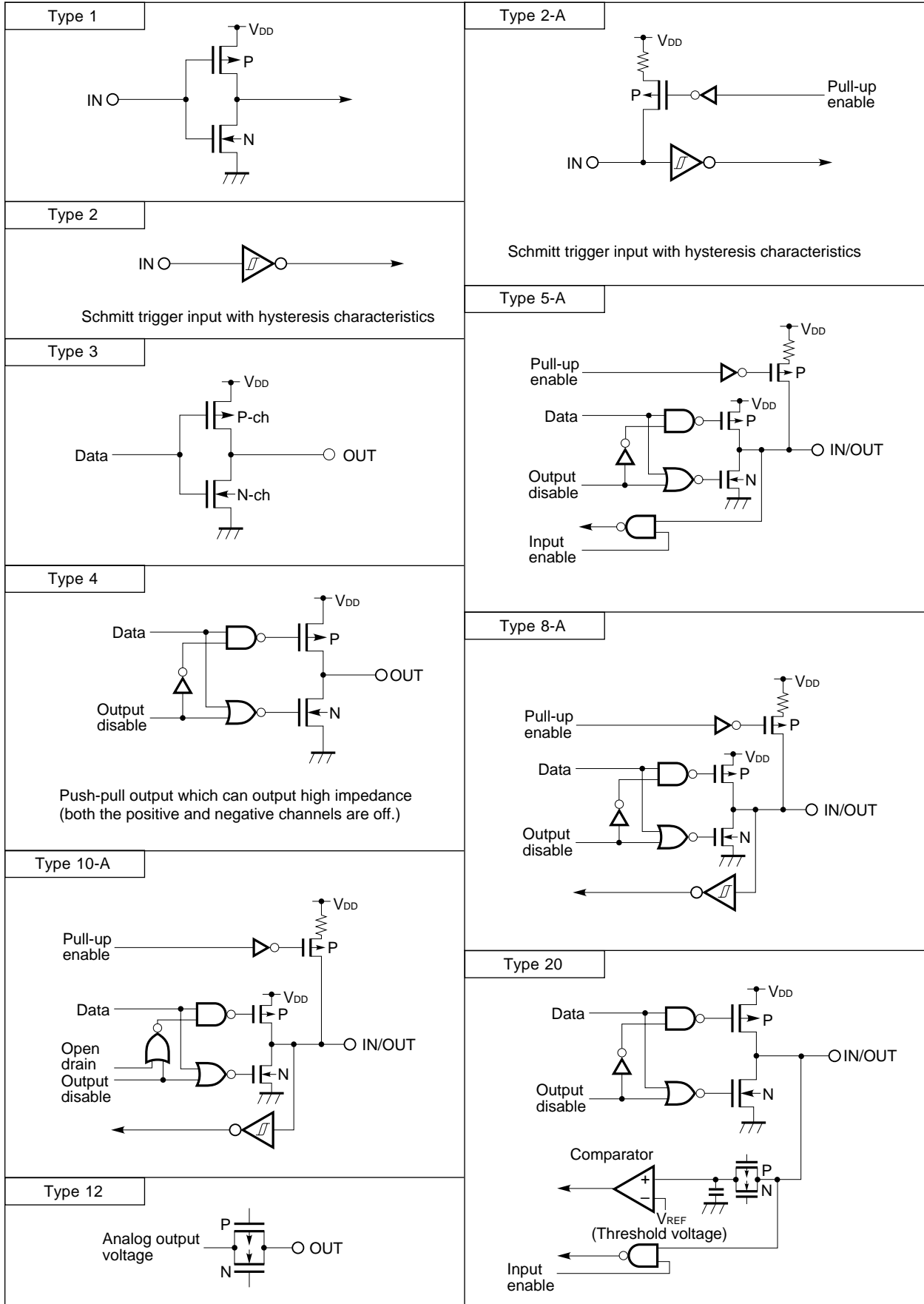
Pin	I/O circuit type	I/O	Recommended connection method for unused pins
RESET	2	Input	—
TEST	1		To be connected to V <sub>SS</sub> directly
XT2	—	—	To be left open
XT1		Input	To be connected to V <sub>SS</sub>
PWM0, PWM1	3	Output	To be left open
R <sub>X</sub>	1	Input	To be connected to V <sub>DD</sub> or V <sub>SS</sub>
T <sub>X</sub>	3	Output	To be left open
AV <sub>REF1</sub>	—	—	To be connected to V <sub>SS</sub>
AV <sub>SS</sub>			
AV <sub>DD</sub>			To be connected to V <sub>DD</sub>

★

**Caution** When the I/O mode of an I/O dual-function pin is unpredictable, connect the pin to V<sub>DD</sub> through a resistor of 10 to 100 kΩ (particularly when the voltage of the reset input pin becomes higher than that of the low level input at power-on or when I/O is switched by software).

**Remark** Since type numbers are consistent in the 78K series, those numbers are not always serial in each product. (Some circuits are not included.)

Figure 4-1. I/O Circuits for Pins



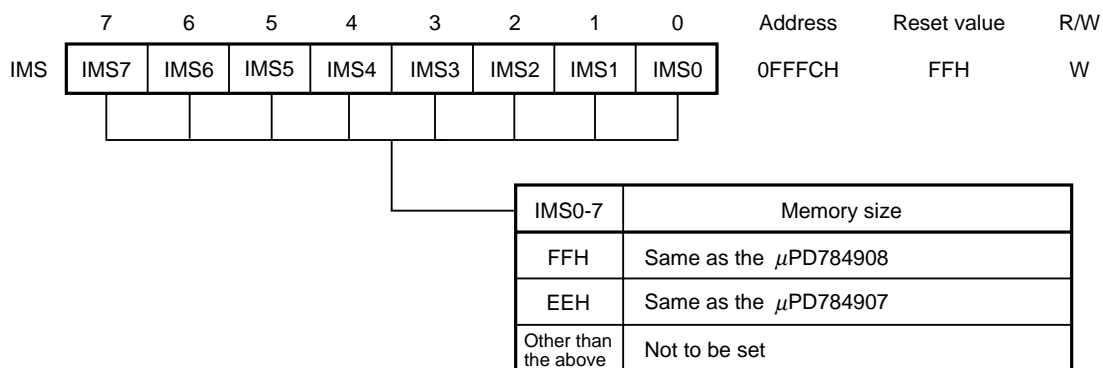
### 5. INTERNAL MEMORY SIZE SELECT REGISTER (IMS)

This register enables the software to avoid using part of the internal memory. The IMS can be set to establish the same memory mapping as used in mask ROM products that have different internal memory (ROM and RAM) configurations.

The IMS is set using 8-bit memory operation instructions.

A  $\overline{\text{RESET}}$  input sets the IMS to FFH.

Figure 5-1. Internal Memory Size Select Register (IMS)



The IMS is not contained in a mask ROM product (μPD784907 or μPD784908). But the action is not affected if the write command to the IMS is executed to the mask ROM product.

## 6. PROM PROGRAMMING

The μPD78P4908 has an on-chip 128-KB PROM device for use as program memory. When programming, set the  $V_{PP}$  and  $\overline{\text{RESET}}$  pins for PROM programming mode. See **2. PIN CONFIGURATION (TOP VIEW) (2) PROM programming mode** with regard to handling of other, unused pins.

### 6.1 OPERATION MODE

PROM programming mode is selected when +6.5 V is added to the  $V_{DD}$  pin, +12.5 V is added to the  $V_{PP}$  pin, or low-level input is added to the  $\overline{\text{RESET}}$  pin. This mode can be set to operation mode by setting the  $\overline{\text{CE}}$  pin,  $\overline{\text{OE}}$  pin, and  $\overline{\text{PGM}}$  pin as shown in Table 6-1 below.

In addition, the PROM contents can be read by setting read mode.

**Table 6-1. PROM Programming Operation Mode**

Pin	$\overline{\text{RESET}}$	$V_{PP}$	$V_{DD}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	D0-D7
Operation mode							
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High impedance
				×	L	L	
Read	L	+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High impedance
Standby				H	×	×	High impedance

**Remark** × = L or H

**(1) Read mode**

Set  $\overline{CE}$  to L and  $\overline{OE}$  to L to set read mode.

**(2) Output disable mode**

Set  $\overline{OE}$  to H to set high impedance for data output and output disable mode.

Consequently, if several  $\mu$ PD78P4908 devices are connected to a data bus, the  $\overline{OE}$  pins can be controlled to select data output from any of the devices.

**(3) Standby mode**

Set  $\overline{CE}$  to H to set standby mode.

In this mode, data output is set to high impedance regardless of the  $\overline{OE}$  setting.

**(4) Page data latch mode**

At the beginning of page write mode, set  $\overline{CE}$  to H,  $\overline{PGM}$  to H, and  $\overline{OE}$  to L to set page data latch mode.

In this mode, 1 page (4 bytes) of data are latched to the internal address/data latch circuit.

**(5) Page write mode**

After latching the address and data for one page (4 bytes) using page data latch mode, adding a 0.1 ms program pulse (active, low) to the  $\overline{PGM}$  pin with both  $\overline{CE}$  and  $\overline{OE}$  set to H causes page write to be executed. Later, setting both  $\overline{CE}$  and  $\overline{OE}$  to L causes program verification to be executed.

If programming is not completed after one program pulse, the write and verify operations may be repeated X times (where  $X \leq 10$ ).

**(6) Byte write mode**

Adding a 0.1 ms program pulse (active, low) to the  $\overline{PGM}$  pin with setting  $\overline{CE}$  to L and  $\overline{OE}$  to H causes byte write to be executed. Later, setting  $\overline{OE}$  to L causes program verification to be executed.

If programming is not completed after one program pulse, the write and verify operations may be repeated X times (where  $X \leq 10$ ).

**(7) Program verify mode**

Set  $\overline{CE}$  to L,  $\overline{PGM}$  to H, and  $\overline{OE}$  to L to set program verify mode. Use verify mode for verification following each write operation.

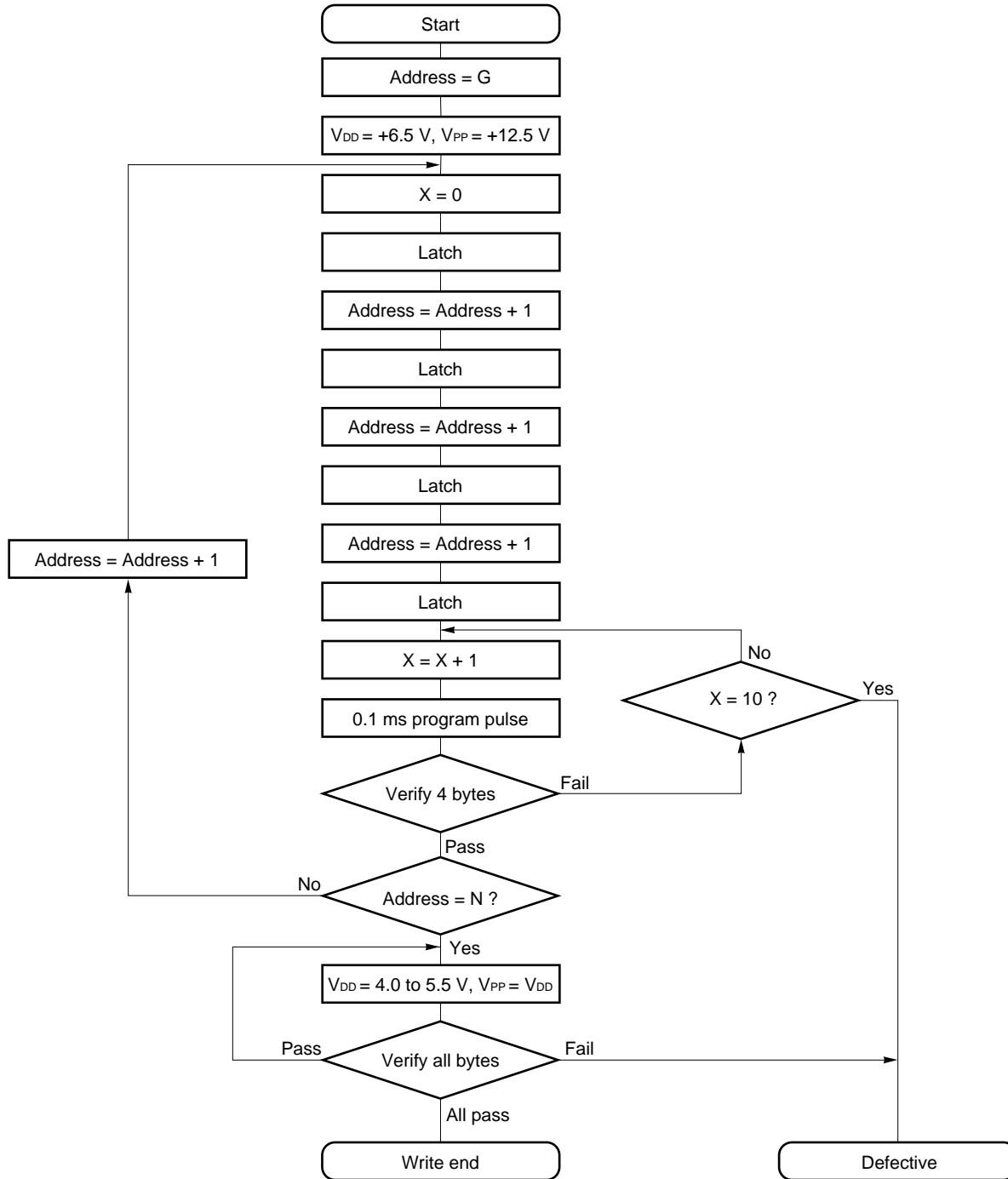
**(8) Program inhibit mode**

Program inhibit mode is used to write to a single device when several  $\mu$ PD78P4908 devices are connected in parallel to  $\overline{OE}$ ,  $V_{PP}$ , and D0 to D7 pins.

Use the page write mode or byte write mode described above for each write operation. Write operations cannot be done for devices in which the  $\overline{PGM}$  pin has been set to H.

6.2 PROM WRITE SEQUENCE

Figure 6-1. Page Program Mode Flowchart



**Remark** G = Start address  
 N = Program end address

Figure 6-2. Page Program Mode Timing

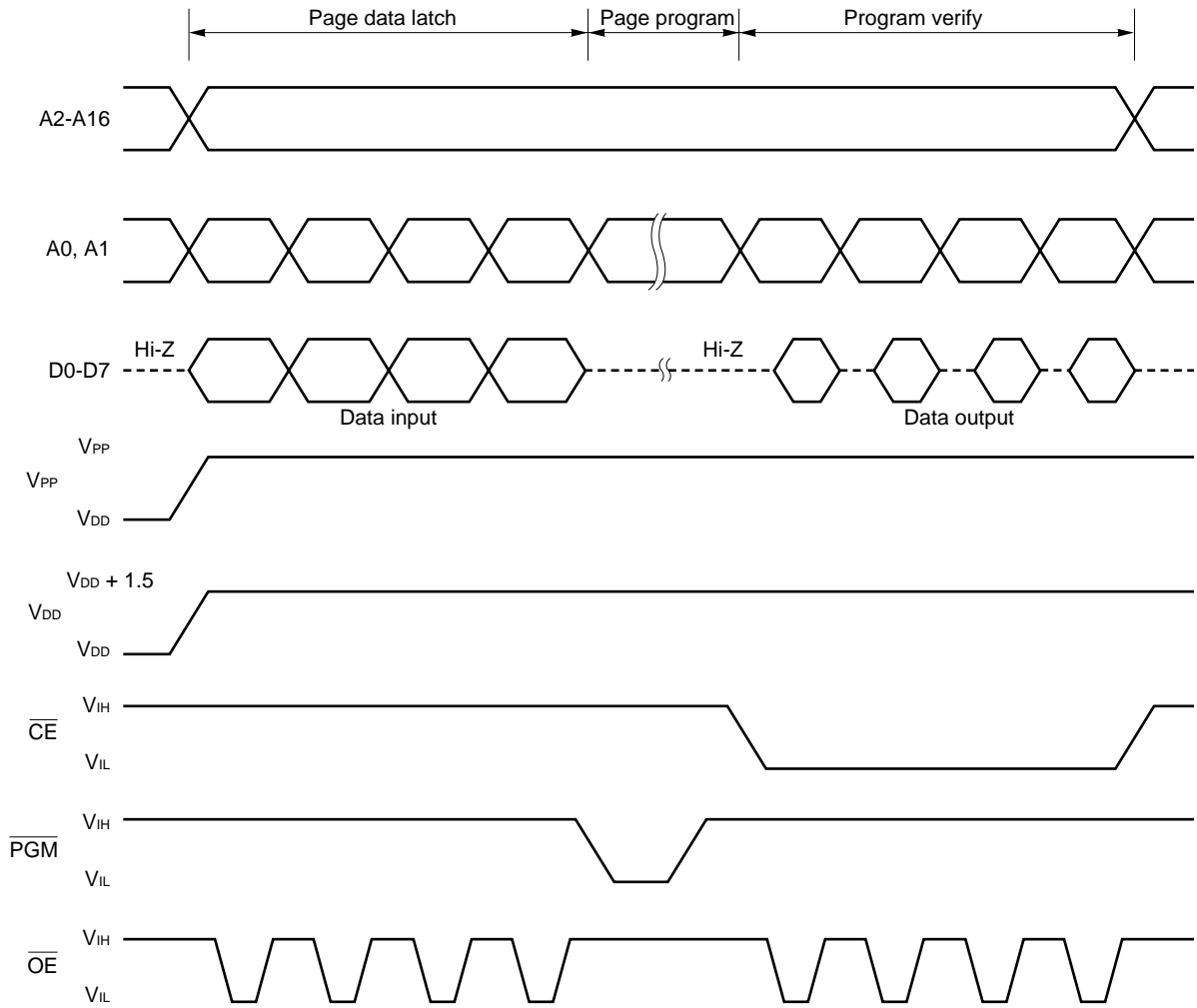
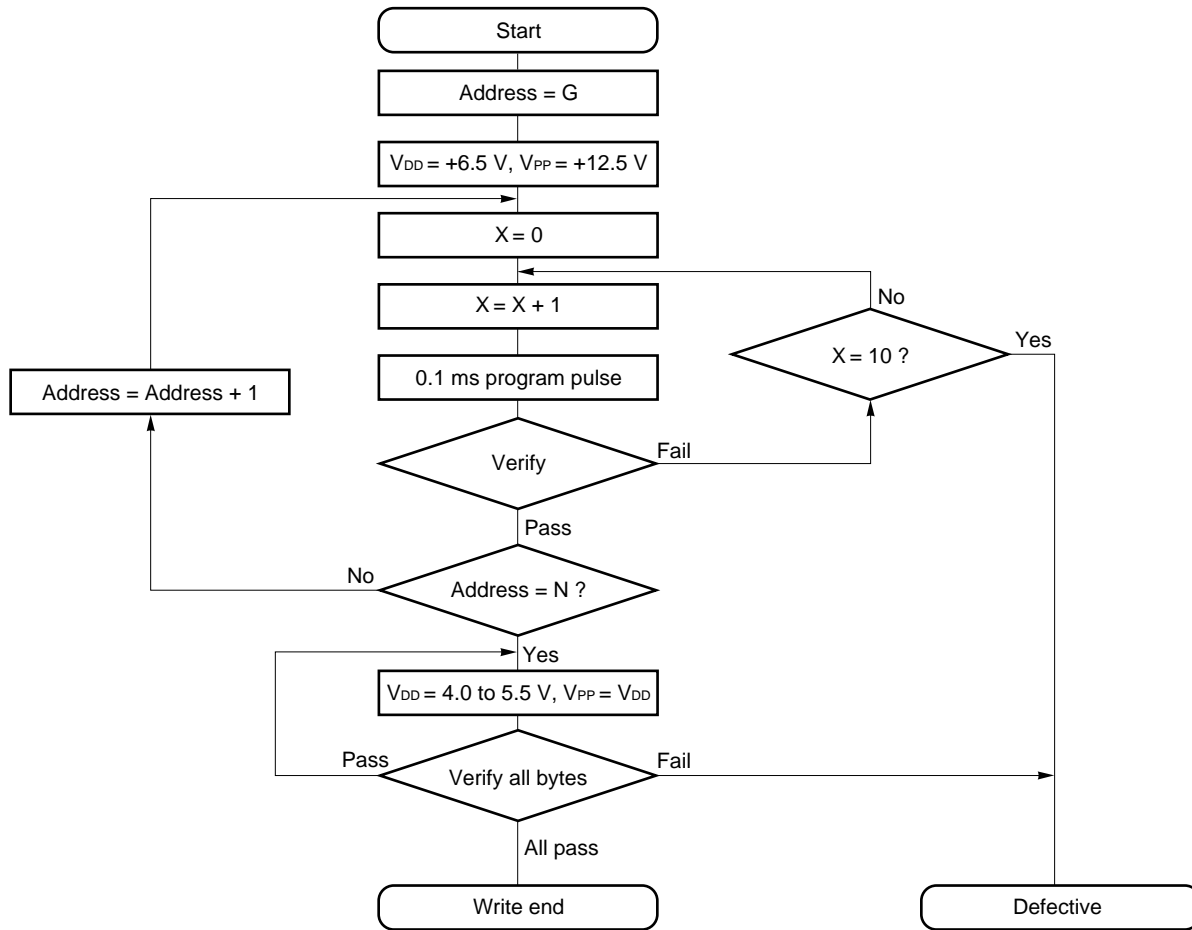


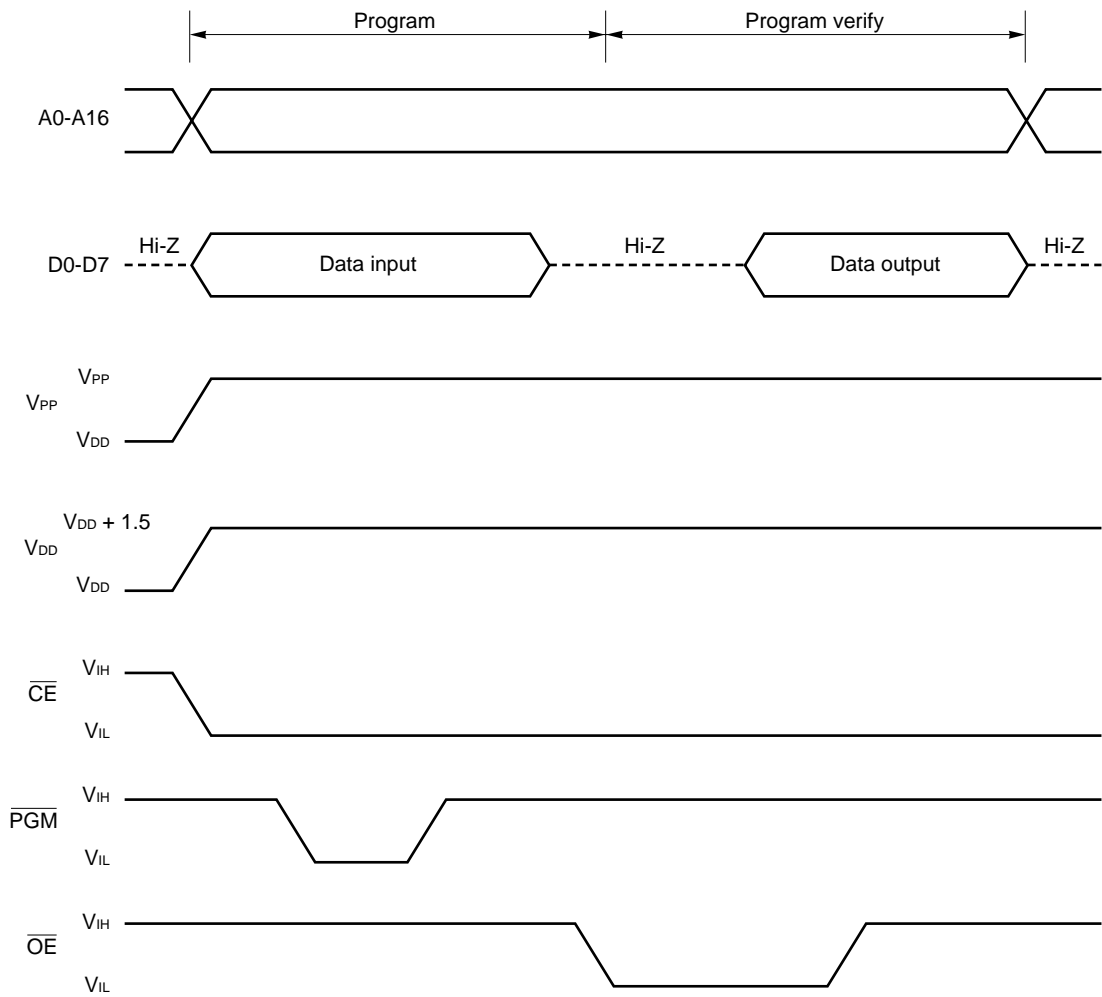
Figure 6-3. Byte Program Mode Flowchart



**Remark** G = Start address  
 N = Program end address



Figure 6-4. Byte Program Mode Timing



- Cautions**
1. Add V<sub>DD</sub> before V<sub>PP</sub>, and turn off the V<sub>DD</sub> after V<sub>PP</sub>.
  2. Do not allow V<sub>PP</sub> to exceed 13.5 V including overshoot.
  3. Reliability problems may result if the device is inserted or pulled out while 12.5 V is applied at V<sub>PP</sub>.

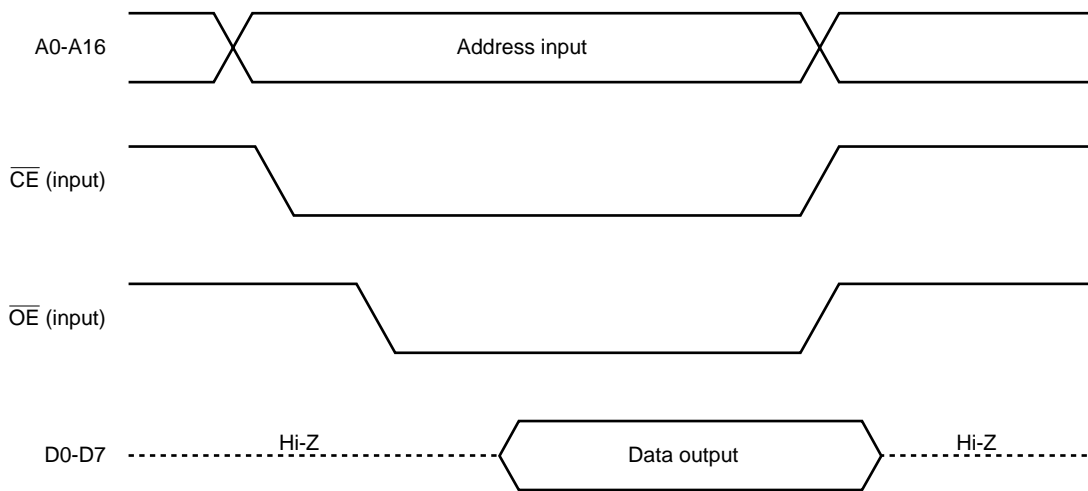
**6.3 PROM READ SEQUENCE**

Follow this sequence to read the PROM contents to an external data bus (D0 to D7).

- (1) Set the  $\overline{\text{RESET}}$  pin to low level and add 5 V to the  $V_{PP}$  pin. See **2. PIN CONFIGURATION (TOP VIEW) (2) PROM programming mode** with regard to handling of other, unused pins.
- (2) Add 5 V to the  $V_{DD}$  and  $V_{PP}$  pins.
- (3) Input the data address to be read to pins A0 to A16.
- (4) Set read mode.
- (5) Output the data to pins D0 to D7.

Figure 6-5 shows the timing of steps (2) to (5) above.

**Figure 6-5. PROM Read Timing**



**7. SCREENING ONE-TIME PROM PRODUCTS**

NEC cannot execute a complete test of one-time PROM products (μPD78P4908GF-3BA) due to their structure before shipment. It is recommended that you screen (verify) PROM products after writing necessary data into them and storing them at 125°C for 24 hours.

8. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V <sub>DD</sub>		-0.3 to +7.0	V
	AV <sub>DD</sub>		-0.3 to V <sub>DD</sub> + 0.3	V
	AV <sub>SS</sub>		-0.3 to +0.3	V
Input voltage	V <sub>I1</sub>	For pins other than V <sub>PP</sub> , A9	-0.3 to V <sub>DD</sub> + 0.3	V
	V <sub>I2</sub>	V <sub>PP</sub> , A9	-0.3 to +13.5	V
Analog input voltage	V <sub>AN</sub>		AV <sub>SS</sub> - 0.3 to AV <sub>REF1</sub> + 0.3	V
Output voltage	V <sub>O</sub>		-0.3 to V <sub>DD</sub> + 0.3	V
Output low current	I <sub>OL</sub>	One pin	10	mA
		Total for the P00-P07, P30-P37, P54-P57, P60-P67, and P100-P107 pins	50	mA
		Total for the P10-P17, P40-P47, P50-P53, P70-P77, P90-P97, PWM0, PWM1, and $\overline{\text{TX}}$ pins	50	mA
Output high current	I <sub>OH</sub>	One pin	-6	mA
		Total for the P00-P07, P30-P37, P54-P57, P60-P67, and P100-P107 pins	-30	mA
		Total for the P10-P17, P40-P47, P50-P53, P70-P77, P90-P97, PWM0, PWM1, and $\overline{\text{TX}}$ pins	-30	mA
A/D converter reference input voltage	AV <sub>REF1</sub>		-0.3 to V <sub>DD</sub> + 0.3	V
Operating ambient temperature	T <sub>A</sub>		-40 to +85	°C
Storage temperature	T <sub>stg</sub>		-65 to +150	°C

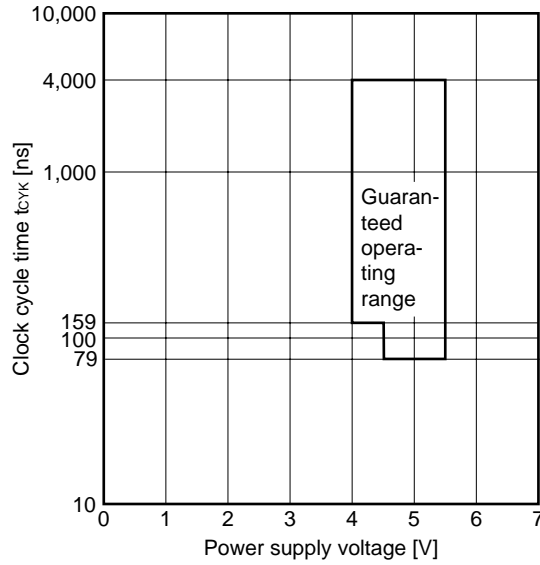
**Caution** Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

**Remark** Unless otherwise stated, the characteristics of a dual-function pin are the same as those of a port pin.

**OPERATING CONDITIONS**

- Operating ambient temperature (T<sub>A</sub>): -40 °C to +85 °C
- Power supply voltage and clock cycle time: See **Figure 8-1**.
- Internal regulator operation selected (REGOFF pin: low level)

**Figure 8-1. Power Supply Voltage and Clock Cycle Time**



**CAPACITANCE (T<sub>A</sub> = 25 °C, V<sub>DD</sub> = V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>i</sub>	f = 1 MHz 0 V on pins other than measured pins			15	pF
Output capacitance	C <sub>o</sub>				15	pF
I/O capacitance	C <sub>io</sub>				15	pF

★ **MAIN OSCILLATOR CHARACTERISTICS (T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Oscillator frequency	f <sub>xx</sub>	Ceramic or crystal resonator	2	12.58	MHz

**Caution** When using the clock generator, run wires according to the following rules to avoid effects such as stray capacitance:

- Minimize the wiring length.
- Never cause the wires to cross other signal lines.
- Never cause the wires to run near a line carrying a large varying current.
- The grounding point of the capacitor of the oscillator circuit must always be the same potential as V<sub>SS1</sub>. Never connect the capacitor to a ground pattern carrying a large current.
- Never extract a signal from the oscillator.

★ **Remark** Connect a 12.582912 or 6.291456 MHz oscillator to operate the internal clock timer with the main clock.

**CLOCK OSCILLATOR CHARACTERISTICS (T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillator frequency	f <sub>XT</sub>	Ceramic or crystal resonator	32	32.768	35	kHz
Oscillation settling time	t <sub>SXT</sub>	V <sub>DD</sub> = 4.5 to 5.5 V		1.2	2	s
					10	s
Oscillation hold voltage	V <sub>BDXT</sub>		4.0		5.5	V
Watch timer operating voltage	V <sub>BDW</sub>		4.0		5.5	V

DC CHARACTERISTICS (T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = AV<sub>DD</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage <sup>Note 5</sup>	V <sub>IL1</sub>	For pins other than those described in <b>Notes 1 and 2</b>	-0.3		0.3 V <sub>DD</sub>	V
	V <sub>IL2</sub>	For pins described in <b>Note 1</b>	-0.3		0.2 V <sub>DD</sub>	V
	V <sub>IL3</sub>	V <sub>DD</sub> = 4.5 to 5.5 V For pins described in <b>Note 2</b>	-0.3		+0.8	V
Input high voltage	V <sub>IH1</sub>	For pins other than those described in <b>Notes 1 and 2</b>	0.7 V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V
	V <sub>IH2</sub>	For pins described in <b>Note 1</b>	0.8 V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V
	V <sub>IH3</sub>	V <sub>DD</sub> = 4.5 to 5.5 V For pins described in <b>Note 2</b>	2.2		V <sub>DD</sub> + 0.3	V
Output low voltage	V <sub>OL1</sub>	I <sub>OL</sub> = 20 μA			0.1	V
		I <sub>OL</sub> = 100 μA			0.2	V
		I <sub>OL</sub> = 2 mA			0.4	V
	V <sub>OL2</sub>	I <sub>OL</sub> = 8 mA For pins described in <b>Note 4</b> V <sub>DD</sub> = 4.5 to 5.5 V			1.0	V
Output high voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -20 μA	V <sub>DD</sub> - 0.1			V
		I <sub>OH</sub> = -100 μA	V <sub>DD</sub> - 0.2			V
		I <sub>OH</sub> = -2 mA	V <sub>DD</sub> - 1.0			V
	V <sub>OH2</sub>	V <sub>DD</sub> = 4.5 to 5.5 V I <sub>OH</sub> = -5 mA For pins described in <b>Note 3</b>	V <sub>DD</sub> - 2.4			V

- Notes 1.** X1, X2,  $\overline{\text{RESET}}$ , P12/ $\overline{\text{ASCK2}}$ / $\overline{\text{SCK2}}$ , P20/ $\overline{\text{NMI}}$ , P21/ $\overline{\text{INTP0}}$ , P22/ $\overline{\text{INTP1}}$ , P23/ $\overline{\text{INTP2}}$ / $\overline{\text{CI}}$ , P24/ $\overline{\text{INTP3}}$ , P25/ $\overline{\text{INTP4}}$ / $\overline{\text{ASCK1}}$ / $\overline{\text{SCK1}}$ , P26/ $\overline{\text{INTP5}}$ , P27/ $\overline{\text{SI0}}$ , P32/ $\overline{\text{SCK0}}$ , P33/ $\overline{\text{SO0}}$ , P105/ $\overline{\text{SCK3}}$ , P106/ $\overline{\text{SI3}}$ , P107/ $\overline{\text{SO3}}$ , XT1, XT2
- 2.** P40/ $\overline{\text{AD0}}$ -P47/ $\overline{\text{AD7}}$ , P50/ $\overline{\text{A8}}$ -P57/ $\overline{\text{A15}}$ , P60/ $\overline{\text{A16}}$ -P67/ $\overline{\text{REFRQ}}$ / $\overline{\text{HLDK}}$ , P00-P07
- 3.** P00-P07
- 4.** P10-P17, P40/ $\overline{\text{AD0}}$ -P47/ $\overline{\text{AD7}}$ , P50/ $\overline{\text{A8}}$ -P57/ $\overline{\text{A15}}$
- 5.** Other than pull-up resistors

DC CHARACTERISTICS (T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = AV<sub>DD</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current	I <sub>LI1</sub>	0 V ≤ V <sub>I</sub> ≤ V <sub>DD</sub>	For pins other than X1 and XT1			±10	μA
	I <sub>LI2</sub>		X1, XT1			±20	μA
Output leakage current	I <sub>LO</sub>	0 V ≤ V <sub>O</sub> ≤ V <sub>DD</sub>				±10	μA
V <sub>DD</sub> supply current <sup>Note</sup>	I <sub>DD1</sub>	Operation mode	f <sub>XX</sub> = 12.58 MHz V <sub>DD</sub> = 4.5 to 5.5 V		20	40	mA
			f <sub>XX</sub> = 6.29 MHz V <sub>DD</sub> = 4.0 to 5.5 V		10	20	mA
	I <sub>DD2</sub>	HALT mode	f <sub>XX</sub> = 12.58 MHz V <sub>DD</sub> = 4.5 to 5.5 V f <sub>CLK</sub> = f <sub>XX</sub> /8 (STBC = B1H) Peripheral operation stops.		5.2	10.4	mA
			f <sub>XX</sub> = 6.29 MHz V <sub>DD</sub> = 4.0 to 5.5 V f <sub>CLK</sub> = f <sub>XX</sub> /8 (STBC = 31H) Peripheral operation stops.		2.6	5.2	mA
	I <sub>DD3</sub>	IDLE mode	f <sub>XX</sub> = 12.58 MHz V <sub>DD</sub> = 4.5 to 5.5 V		2.4	4.8	mA
			f <sub>XX</sub> = 6.29 MHz V <sub>DD</sub> = 4.0 to 5.5 V		1.8	3.6	mA
Pull-up resistor	R <sub>L</sub>	V <sub>I</sub> = 0 V		15		80	kΩ

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**Note** These values are valid when the internal regulator is ON (REGOFF pin = low level). They do not include the AV<sub>DD</sub> and AV<sub>REF1</sub> currents.

AC CHARACTERISTICS (T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = AV<sub>DD</sub> = 4.0 to 5.5 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0 V)

(1) Read/write operation

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Address setup time (to ASTB↓)	t <sub>SAST</sub>	V <sub>DD</sub> = 5.0 V	(0.5 + a)T - 11	29		ns
ASTB high-level width	t <sub>WSTH</sub>	V <sub>DD</sub> = 5.0 V	(0.5 + a)T - 17	23		ns
Address hold time (to ASTB↓)	t <sub>HSTLA</sub>	V <sub>DD</sub> = 5.0 V	0.5T - 19	21		ns
Address hold time (to $\overline{RD}\uparrow$ )	t <sub>HRA</sub>	V <sub>DD</sub> = 5.0 V	0.5T - 14	26		ns
Delay from address to $\overline{RD}\downarrow$	t <sub>DAR</sub>	V <sub>DD</sub> = 5.0 V	(1 + a)T - 5	74		ns
Address float time (to $\overline{RD}\downarrow$ )	t <sub>FRA</sub>			0		ns
Delay from address to data input	t <sub>DAID</sub>	V <sub>DD</sub> = 5.0 V	(2.5 + a + n)T - 37		400	ns
Delay from ASTB↓ to data input	t <sub>DSTID</sub>	V <sub>DD</sub> = 5.0 V	(2 + n)T - 35		283	ns
Delay from $\overline{RD}\downarrow$ to data input	t <sub>DRID</sub>	V <sub>DD</sub> = 5.0 V	(1.5 + n)T - 40		238	ns
Delay from ASTB↓ to $\overline{RD}\downarrow$	t <sub>DSTR</sub>	V <sub>DD</sub> = 5.0 V	0.5T - 9	31		ns
Data hold time (to $\overline{RD}\uparrow$ )	t <sub>HRID</sub>			0		ns
Delay from $\overline{RD}\uparrow$ to address active	t <sub>DRA</sub>	V <sub>DD</sub> = 5.0 V	0.5T - 2	38		ns
Delay from $\overline{RD}\uparrow$ to ASTB↑	t <sub>DRST</sub>	V <sub>DD</sub> = 5.0 V	0.5T - 9	31		ns
$\overline{RD}$ low-level width	t <sub>WRL</sub>	V <sub>DD</sub> = 5.0 V	(1.5 + n)T - 25	94		ns
Delay from address↓ to $\overline{WR}\downarrow$	t <sub>DAW</sub>	V <sub>DD</sub> = 5.0 V	(1 + a)T - 5	74		ns
Address hold time (to $\overline{WR}\uparrow$ )	t <sub>HWA</sub>	V <sub>DD</sub> = 5.0 V	0.5T - 14	26		ns
Delay from ASTB↓ to data output	t <sub>DSTOD</sub>	V <sub>DD</sub> = 5.0 V	0.5T + 15		55	ns
Delay from $\overline{WR}\downarrow$ to data output	t <sub>DWOD</sub>				15	ns
Delay from ASTB↓ to $\overline{WR}\downarrow$	t <sub>DSTW</sub>	V <sub>DD</sub> = 5.0 V	0.5T - 9	31		ns
Data setup time (to $\overline{WR}\uparrow$ )	t <sub>SODWR</sub>	V <sub>DD</sub> = 5.0 V	(1.5 + n)T - 20	99		ns
Data hold time (to $\overline{WR}\uparrow$ )	t <sub>HWOD</sub>	V <sub>DD</sub> = 5.0 V	0.5T - 14	26		ns
Delay from $\overline{WR}\uparrow$ to ASTB↑	t <sub>DWST</sub>	V <sub>DD</sub> = 5.0 V	0.5T - 9	31		ns
$\overline{WR}$ low-level width	t <sub>WWL</sub>	V <sub>DD</sub> = 5.0 V	(1.5 + n)T - 25	94		ns

**Remark** T: t<sub>CYK</sub> (system clock cycle time) V<sub>DD</sub> = 5.0 V T = 79 ns (MIN.)

a: 1 during address wait, otherwise, 0

n: Number of wait states (n ≥ 0)



(2) External wait timing

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Delay from address to $\overline{\text{WAIT}}\downarrow$ input	t <sub>DAWT</sub>	V <sub>DD</sub> = 5.0 V	(2 + a)T - 40		198	ns
Delay from ASTB $\downarrow$ to $\overline{\text{WAIT}}\downarrow$ input	t <sub>DSTWT</sub>	V <sub>DD</sub> = 5.0 V	1.5T - 40		79	ns
Hold time from ASTB $\downarrow$ to $\overline{\text{WAIT}}$	t <sub>HSTWT</sub>	V <sub>DD</sub> = 5.0 V	(0.5 + n)T + 5	124		ns
Delay from ASTB $\downarrow$ to $\overline{\text{WAIT}}\uparrow$	t <sub>DSTWTH</sub>	V <sub>DD</sub> = 5.0 V	(1.5 + n)T - 40		238	ns
Delay from $\overline{\text{RD}}\downarrow$ to $\overline{\text{WAIT}}\downarrow$ input	t <sub>DRWTL</sub>	V <sub>DD</sub> = 5.0 V	T - 40		39	ns
Hold time from $\overline{\text{RD}}\downarrow$ to $\overline{\text{WAIT}}$	t <sub>HRWT</sub>	V <sub>DD</sub> = 5.0 V	nT + 5	84		ns
Delay from $\overline{\text{RD}}\downarrow$ to $\overline{\text{WAIT}}\uparrow$	t <sub>DRWTH</sub>	V <sub>DD</sub> = 5.0 V	(1 + n)T - 40		198	ns
Delay from $\overline{\text{WAIT}}\uparrow$ to data input	t <sub>DWTID</sub>	V <sub>DD</sub> = 5.0 V	0.5T - 5		35	ns
Delay from $\overline{\text{WAIT}}\uparrow$ to $\overline{\text{RD}}\uparrow$	t <sub>DWTR</sub>	V <sub>DD</sub> = 5.0 V	0.5T	40		ns
Delay from $\overline{\text{WAIT}}\uparrow$ to $\overline{\text{WR}}\uparrow$	t <sub>DWTW</sub>	V <sub>DD</sub> = 5.0 V	0.5T	40		ns
Delay from $\overline{\text{WR}}\downarrow$ to $\overline{\text{WAIT}}\downarrow$ input	t <sub>DWWTL</sub>	V <sub>DD</sub> = 5.0 V	T - 40		39	ns
Hold time from $\overline{\text{WR}}\downarrow$ to $\overline{\text{WAIT}}$	t <sub>HWWT</sub>	V <sub>DD</sub> = 5.0 V	nT + 5	84		ns
Delay from $\overline{\text{WR}}\downarrow$ to $\overline{\text{WAIT}}\uparrow$	t <sub>DWWTH</sub>	V <sub>DD</sub> = 5.0 V	(1 + n)T - 40		198	ns

**Remark** T: t<sub>CYK</sub> (system clock cycle time) V<sub>DD</sub> = 5.0 V T = 79 ns (MIN.)  
 a: 1 during address wait, otherwise, 0  
 n: Number of wait states (n ≥ 0)

**(3) Bus hold timing**

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Delay from HLDRQ↑ to float	t <sub>FHQC</sub>	V <sub>DD</sub> = 5.0 V	(2 + 4 + a + n)T + 50		765	ns
Delay from HLDRQ↑ to HLDAC↑	t <sub>DHQHHAH</sub>	V <sub>DD</sub> = 5.0 V	(3 + 4 + a + n)T + 30		825	ns
Delay from float to HLDAC↑	t <sub>DCFHA</sub>	V <sub>DD</sub> = 5.0 V	T + 30		109	ns
Delay from HLDRQ↓ to HLDAC↓	t <sub>DHQLHAL</sub>	V <sub>DD</sub> = 5.0 V	2T + 40		199	ns
Delay from HLDRQ↓ to active	t <sub>DHAC</sub>	V <sub>DD</sub> = 5.0 V	T - 20	59		ns

**Remark** T: t<sub>CYK</sub> (system clock cycle time) V<sub>DD</sub> = 5.0 V T = 79 ns (MIN.)

a: 1 during address wait, otherwise, 0

n: Number of wait states (n ≥ 0)

**(4) Refresh timing**

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Random read/write cycle time	t <sub>RC</sub>	V <sub>DD</sub> = 5.0 V	3T	238		ns
REFRQ low-level pulse width	t <sub>WRFQL</sub>	V <sub>DD</sub> = 5.0 V	1.5T - 25	94		ns
Delay from ASTB↓ to REFRQ	t <sub>DSTRFQ</sub>	V <sub>DD</sub> = 5.0 V	0.5T - 9	31		ns
Delay from RD↑ to REFRQ	t <sub>DRRFQ</sub>	V <sub>DD</sub> = 5.0 V	1.5T - 9	110		ns
Delay from WR↑ to REFRQ	t <sub>DWRFQ</sub>	V <sub>DD</sub> = 5.0 V	1.5T - 9	110		ns
Delay from REFRQ↑ to ASTB	t <sub>DRFQST</sub>	V <sub>DD</sub> = 5.0 V	0.5T - 9	31		ns
REFRQ high-level pulse width	t <sub>WRFQH</sub>	V <sub>DD</sub> = 5.0 V	1.5T - 25	94		ns

**Remark** T: t<sub>CYK</sub> (system clock cycle time) V<sub>DD</sub> = 5.0 V T = 79 ns (MIN.)

SERIAL OPERATION (T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = 4.0 to 5.5 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0 V)

(1) CSI, CSI3

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Serial clock cycle time ( $\overline{\text{SCK0}}$ , $\overline{\text{SCK3}}$ )	t <sub>CYSK0</sub>	Input	f <sub>CLK</sub> = f <sub>XX</sub>	8/f <sub>XX</sub>		ns
			Other than f <sub>CLK</sub> = f <sub>XX</sub>	4/f <sub>CLK</sub>		ns
		Output	Other than f <sub>CLK</sub> = f <sub>XX</sub> /8	8/f <sub>XX</sub>		ns
			f <sub>CLK</sub> = f <sub>XX</sub> /8	16/f <sub>XX</sub>		ns
Serial clock low-level width ( $\overline{\text{SCK0}}$ , $\overline{\text{SCK3}}$ )	t <sub>WSKL0</sub>	Input	f <sub>CLK</sub> = f <sub>XX</sub>	4/f <sub>XX</sub> - 40		ns
			Other than f <sub>CLK</sub> = f <sub>XX</sub>	2/f <sub>CLK</sub> - 40		
		Output	Other than f <sub>CLK</sub> = f <sub>XX</sub> /8	4/f <sub>XX</sub> - 40		μs
			f <sub>CLK</sub> = f <sub>XX</sub> /8	8/f <sub>XX</sub> - 40		
Serial clock high-level width ( $\overline{\text{SCK0}}$ , $\overline{\text{SCK3}}$ )	t <sub>WSKH0</sub>	Input	f <sub>CLK</sub> = f <sub>XX</sub>	4/f <sub>XX</sub> - 40		ns
			Other than f <sub>CLK</sub> = f <sub>XX</sub>	2/f <sub>CLK</sub> - 40		
		Output	Other than f <sub>CLK</sub> = f <sub>XX</sub> /8	4/f <sub>XX</sub> - 40		μs
			f <sub>CLK</sub> = f <sub>XX</sub> /8	8/f <sub>XX</sub> - 40		
Setup time for SI0, SI3 (to $\overline{\text{SCK0}}$ , $\overline{\text{SCK3}}$ ↑)	t <sub>SSK0</sub>			80		ns
Hold time for SI0, SI3 (to $\overline{\text{SCK0}}$ , $\overline{\text{SCK3}}$ ↑)	t <sub>HSSK0</sub>	External clock		1/f <sub>CLK</sub> + 80		ns
		Internal clock		80		
Output delay time for SO0, SO3 (to $\overline{\text{SCK0}}$ , $\overline{\text{SCK3}}$ ↓)	t <sub>DSBSK1</sub>	CMOS push-pull output	External clock	0	1/f <sub>CLK</sub> + 150	ns
			Internal clock	0	150	ns
	t <sub>DSBSK2</sub>	Open-drain output R <sub>L</sub> = 1 kΩ	External clock	0	1/f <sub>CLK</sub> + 400	ns
			Internal clock	0	400	ns
Output hold time for SO0, SO3 (to $\overline{\text{SCK0}}$ , $\overline{\text{SCK3}}$ ↑)	t <sub>HSBSK</sub>	When data is transferred		0.5t <sub>CYSK0</sub> - 40		ns

**Remarks 1.** The values in this table are those when f<sub>XX</sub> = 12.58 MHz, C<sub>L</sub> is 100 pF.

**2.** f<sub>CLK</sub>: System clock frequency (selectable from f<sub>XX</sub>, f<sub>XX</sub>/2, f<sub>XX</sub>/4, and f<sub>XX</sub>/8 by the standby control register (STBC))

★ **3.** f<sub>XX</sub> : Oscillation frequency (f<sub>XX</sub> = 12.58 MHz or f<sub>XX</sub> = 6.29 MHz)

**(2) IOE1, IOE2 (T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = AV<sub>DD</sub> = 4.0 to 5.5 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Serial clock cycle time ( $\overline{\text{SCK1}}$ , $\overline{\text{SCK2}}$ )	t <sub>CYSK1</sub>	Input	V <sub>DD</sub> = 4.5 to 5.5 V	640		ns
				1,280		ns
		Output	Internal, divided by 8	T		ns
Serial clock low-level width ( $\overline{\text{SCK1}}$ , $\overline{\text{SCK2}}$ )	t <sub>WSKL1</sub>	Input	V <sub>DD</sub> = 4.5 to 5.5 V	280		ns
				600		ns
		Output	Internal, divided by 8	0.5T – 40		ns
Serial clock high-level width ( $\overline{\text{SCK1}}$ , $\overline{\text{SCK2}}$ )	t <sub>WSKH1</sub>	Input	V <sub>DD</sub> = 4.5 to 5.5 V	280		ns
				600		ns
		Output	Internal, divided by 8	0.5T – 40		ns
Setup time for SI1 and SI2 (to $\overline{\text{SCK1}}$ , $\overline{\text{SCK2}}\uparrow$ )	t <sub>SSSK1</sub>			40		ns
Hold time for SI1 and SI2 (to $\overline{\text{SCK1}}$ , $\overline{\text{SCK2}}\uparrow$ )	t <sub>HSSK1</sub>			40		ns
Output delay time for SO1 and SO2 (to $\overline{\text{SCK1}}$ , $\overline{\text{SCK2}}\downarrow$ )	t <sub>DOSK</sub>			0	50	ns
Output hold time for SO1 and SO2 (to $\overline{\text{SCK1}}$ , $\overline{\text{SCK2}}\uparrow$ )	t <sub>HOSK</sub>	When data is transferred		0.5t <sub>CYSK1</sub> – 40		ns

**Remarks 1.** The values in this table are those when C<sub>L</sub> is 100 pF.

**2.** T: Serial clock cycle set by software. The minimum value is 8/f<sub>xx</sub>.

**(3) UART, UART2 (T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = AV<sub>DD</sub> = 4.0 to 5.5 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASCK clock input cycle time	t <sub>CYASK</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	160		ns
			320		ns
ASCK clock low-level width	t <sub>WASKL</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	65		ns
			120		ns
ASCK clock high-level width	t <sub>WASKH</sub>	V <sub>DD</sub> = 4.5 to 5.5 V	65		ns
			120		ns

**CLOCK OUTPUT OPERATION (T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = AV<sub>DD</sub> = 4.0 to 5.5 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
CLKOUT cycle time	t <sub>CYCL</sub>	nT	79	32,000	ns
CLKOUT low-level width	t <sub>CLL</sub>	V <sub>DD</sub> = 4.5 to 5.5 V, 0.5T – 10	30		ns
		0.5T – 20	20		ns
CLKOUT high-level width	t <sub>CLH</sub>	V <sub>DD</sub> = 4.5 to 5.5 V, 0.5T – 10	30		ns
		0.5T – 20	20		ns
★ CLKOUT rise time	t <sub>CLR</sub>	4.5 V ≤ V <sub>DD</sub> < 5.5 V		10	ns
		4.0 V ≤ V <sub>DD</sub> < 4.5 V		20	ns
★ CLKOUT fall time	t <sub>CLF</sub>	4.5 V ≤ V <sub>DD</sub> < 5.5 V		10	ns
		4.0 V ≤ V <sub>DD</sub> < 4.5 V		20	ns

**Remark** n: Dividing ratio set by software in the CPU (n = 1, 2, 4, 8, and 16)

T: t<sub>CYK</sub> (system clock cycle time)

**OTHER OPERATIONS (T<sub>A</sub> = -40 °C to +85 °C, V<sub>DD</sub> = AV<sub>DD</sub> = 4.0 to 5.5 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI low-level width	t <sub>WNIL</sub>		10		μs
NMI high-level width	t <sub>WNIH</sub>		10		μs
INTP0 low-level width	t <sub>WIT0L</sub>		4 t <sub>CYSMP</sub>		ns
INTP0 high-level width	t <sub>WIT0H</sub>		4 t <sub>CYSMP</sub>		ns
Low-level width for INTP1-INTP3 and CI	t <sub>WIT1L</sub>		4 t <sub>CYCPU</sub>		ns
High-level width for INTP1-INTP3 and CI	t <sub>WIT1H</sub>		4 t <sub>CYCPU</sub>		ns
Low-level width for INTP4 and INTP5	t <sub>WIT2L</sub>		10		μs
High-level width for INTP4 and INTP5	t <sub>WIT2H</sub>		10		μs
RESET low-level width <sup>Note</sup>	t <sub>WRSL</sub>		10		μs
RESET high-level width	t <sub>WRSH</sub>		10		μs

**Note** Use the RESET low-level width to ensure the lapse of the oscillation settling time when the power is applied.

**Remark** t<sub>CYSMP</sub>: Sampling clock set by software

t<sub>CYCPU</sub>: CPU operation clock set by software in the CPU

**A/D CONVERTER CHARACTERISTICS** ( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ,  $V_{DD} = AV_{DD} = AV_{REF1} = 4.0$  to  $5.5\text{ V}$ ,  $AV_{SS} = V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8			bit
Total error <sup>Note</sup>		IEAD = 00H	FR = 0		0.6	%
			FR = 1		1.5	%
		IEAD = 01H	$V_{DD} = 4.5$ to $5.5\text{ V}$		1	2.2
Quantization error					$\pm 1/2$	LSB
Conversion time	$t_{CONV}$	FR = 1 $120/f_{CLK}$	9.5		480	$\mu\text{s}$
		FR = 0 $240/f_{CLK}$	19.1		960	$\mu\text{s}$
Sampling time	$t_{SAMP}$	FR = 1 $18/f_{CLK}$	1.4		72	$\mu\text{s}$
		FR = 0 $36/f_{CLK}$	2.9		144	$\mu\text{s}$
Analog input impedance	$R_{AN}$			1,000		$\text{M}\Omega$
$AV_{REF1}$ impedance	$R_{REF1}$		3	10		$\text{k}\Omega$
$AV_{DD}$ power supply voltage	$AI_{DD1}$	CS = 1		2.0	5.0	mA
	$AI_{DD2}$	CS = 0, STOP mode		1.0	20	$\mu\text{A}$

**Note** Quantization error is not included. This parameter is indicated as the ratio to the full-scale value.

**Caution** To execute the conversion by the A/D converter set port 7, multiplexed with the A/D input lines, to output mode to prevent data from being inverted.

**Remark**  $f_{CLK}$ : System clock frequency (selectable from  $f_{XX}$ ,  $f_{XX}/2$ ,  $f_{XX}/4$ , and  $f_{XX}/8$  by the standby control register (STBC))

**IEBus CONTROLLER CHARACTERISTICS** ( $T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ,  $V_{DD} = AV_{DD} = AV_{REF1} = 4.5$  to  $5.5\text{ V}$ ,  $AV_{SS} = V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IEBus standard frequency <sup>Note 1</sup>	$f_s$	Transfer speed: mode 1	6.20	6.29	6.39	MHz
Driver delay time (delay from $\overline{\text{TX}}$ output to bus line) <sup>Note 2</sup>	$t_{DTX}$	$C_L = 50\text{ pF}$ <sup>Note 3</sup>			1.5	$\mu\text{s}$
Receiver delay time (delay from bus line to $\overline{\text{RX}}$ output) <sup>Note 2</sup>	$t_{DRX}$				0.7	$\mu\text{s}$
Transmission delay on bus <sup>Note 2</sup>	$t_{DBUS}$				0.85	$\mu\text{s}$

**Notes 1.** The value conforms to the IEBus standard. The IEBus controller is operable within the range of the oscillator frequency of oscillator characteristics.

**2.** The value is measured when IEBus system clock:  $f_x = 6.29\text{ MHz}$ .

**3.**  $C_L$  is the load capacitance of  $\overline{\text{TX}}$  output line.

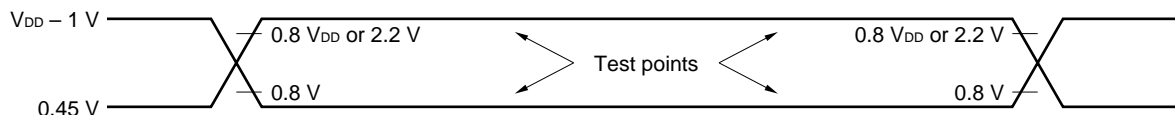
**DATA RETENTION CHARACTERISTICS (T<sub>A</sub> = -40 °C to +85 °C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V <sub>DDDR</sub>	STOP mode	2.5		5.5	V
Data retention current	I <sub>DDDR</sub>	STOP mode V <sub>DDDR</sub> = 2.5 V, AV <sub>REF</sub> = 0 V <sup>Note 1</sup>		2	10	μA
			V <sub>DDDR</sub> = 4.0 to 5.5 V, AV <sub>REF1</sub> = 0 V <sup>Note 1</sup>		10	50
V <sub>DD</sub> rise time	t <sub>rVD</sub>		200			μs
V <sub>DD</sub> fall time	t <sub>fVD</sub>		200			μs
V <sub>DD</sub> hold time (to STOP mode setting)	t <sub>HVD</sub>		0			ms
STOP clear signal input time	t <sub>DREL</sub>		0			ms
Oscillation settling time	t <sub>WAIT</sub>	Crystal resonator	30			ms
		Ceramic resonator	5		0.1 V <sub>DDDR</sub>	ms
Input low voltage	V <sub>IL</sub>	Specific pins <sup>Note 2</sup>	0		V <sub>DDDR</sub>	V
Input high voltage	V <sub>IH</sub>		0.9 V <sub>DDDR</sub>			V

★

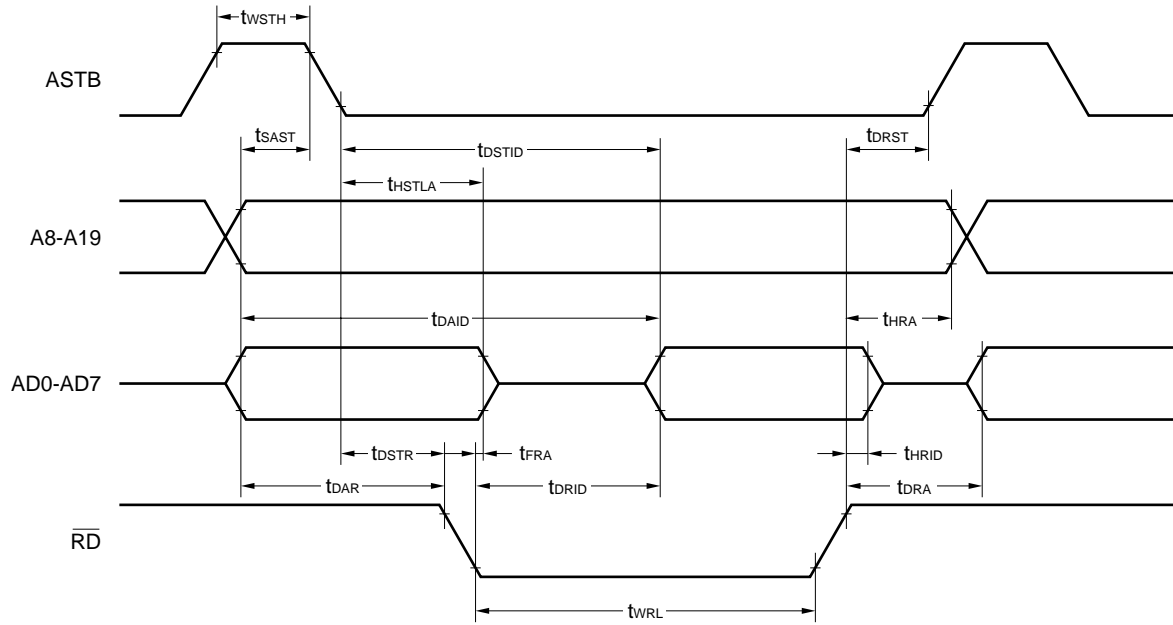
- Notes**
- Valid when input voltages to the pins described in Note 2 satisfy V<sub>IL</sub> or V<sub>IH</sub> in the above table.
  - RESET, P12/ASCK2/SCK2, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK/SCK1, P26/INTP5, P27/SI0, P32/SCK0, P33/SO0, P105/SCK3, P106/SI3, and P107/SO3 pins

**AC TIMING TEST POINTS**

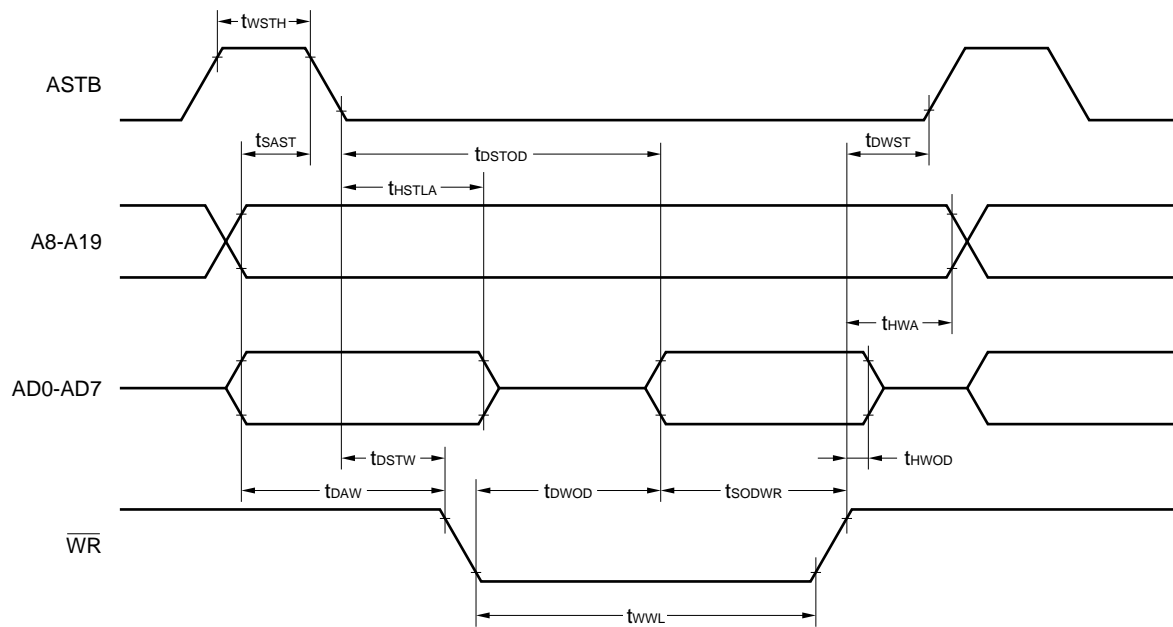


TIMING WAVEFORM

(1) Read operation

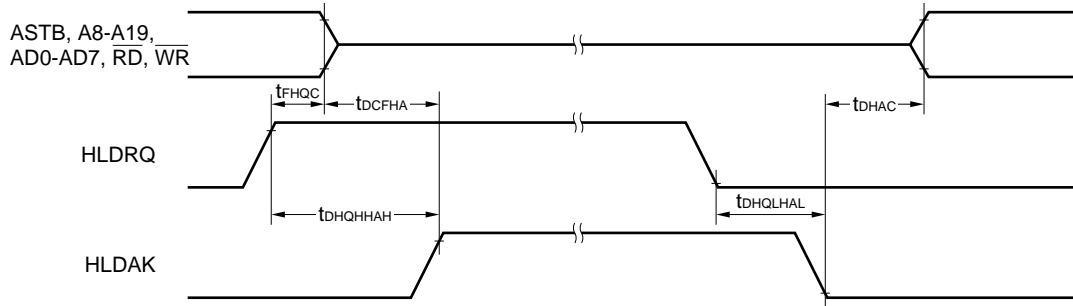


(2) Write operation



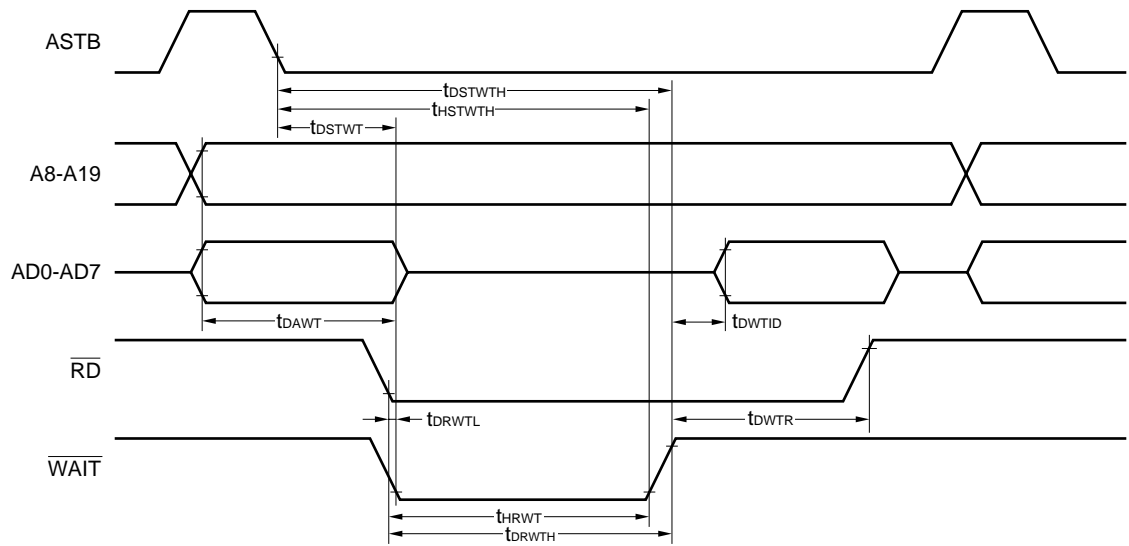


**HOLD TIMING**

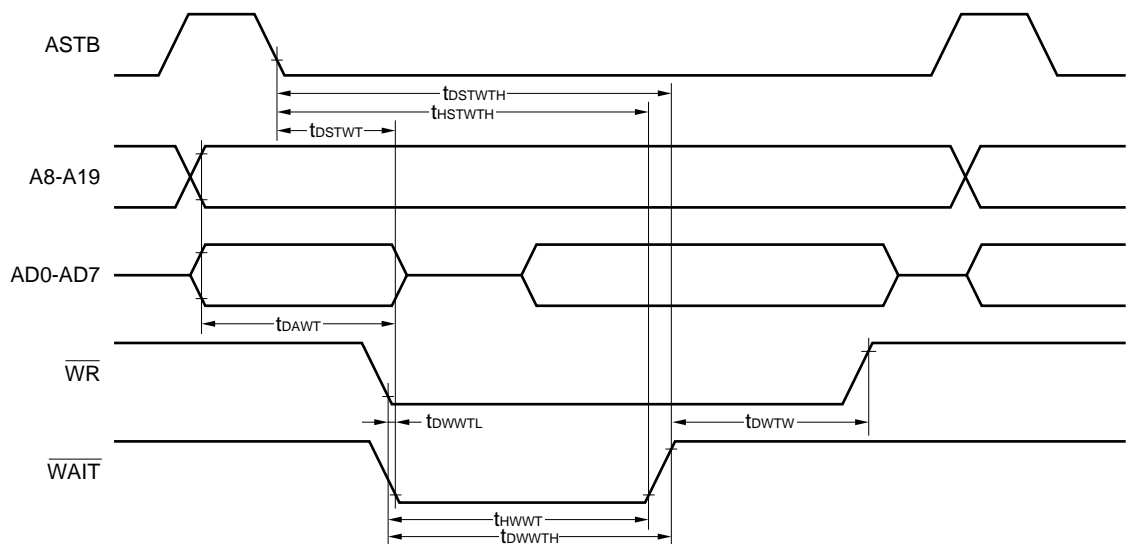


**EXTERNAL WAIT SIGNAL INPUT TIMING**

**(1) Read operation**

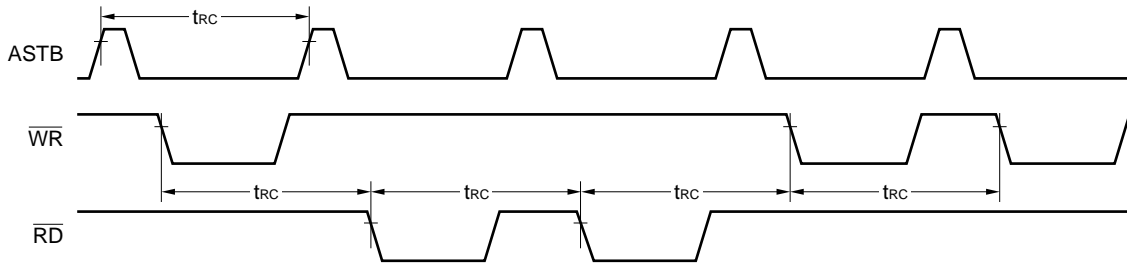


**(2) Write operation**

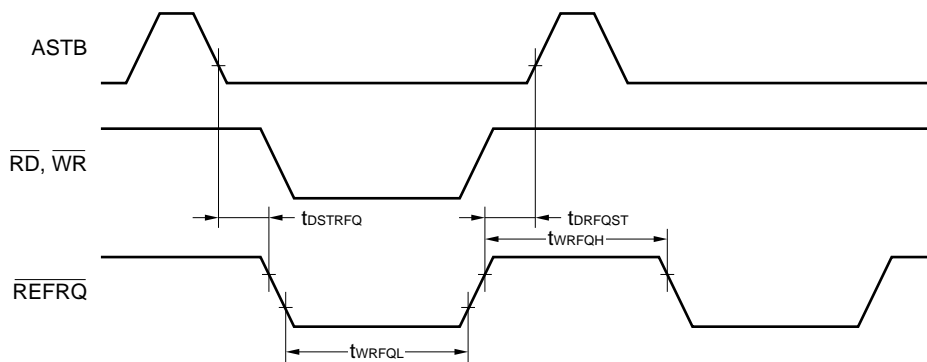


REFRESH TIMING WAVEFORM

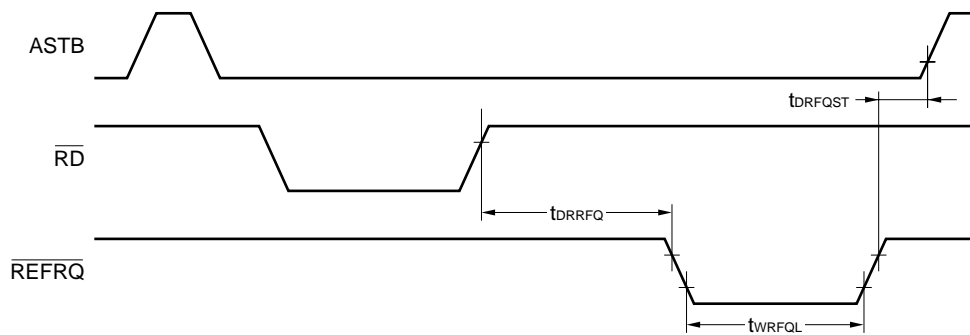
(1) Random read/write cycle



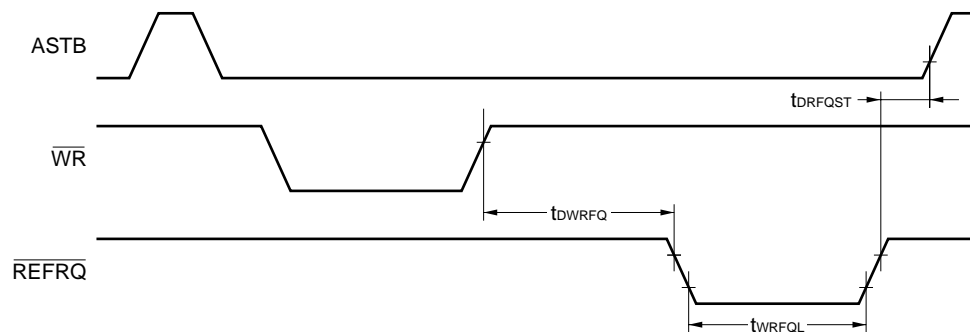
(2) When refresh memory is accessed for a read and write at the same time



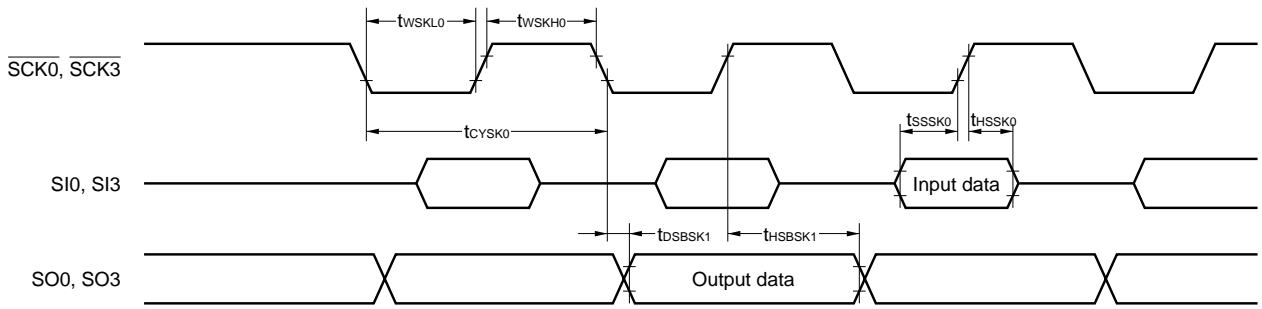
(3) Refresh after a read



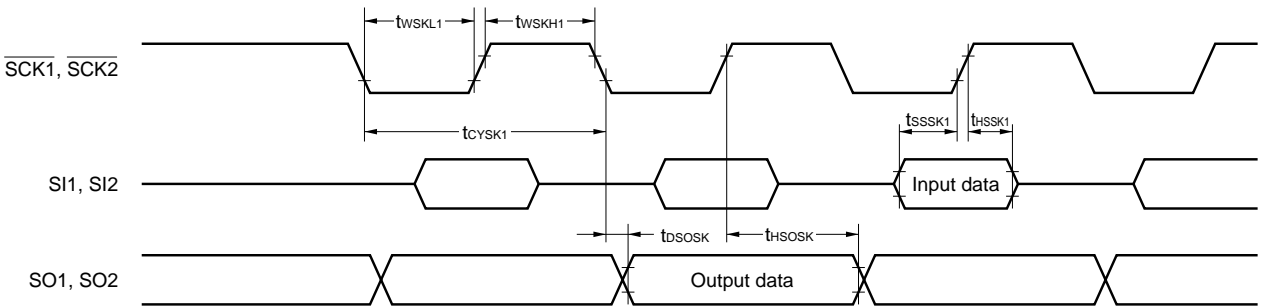
(4) Refresh after a write



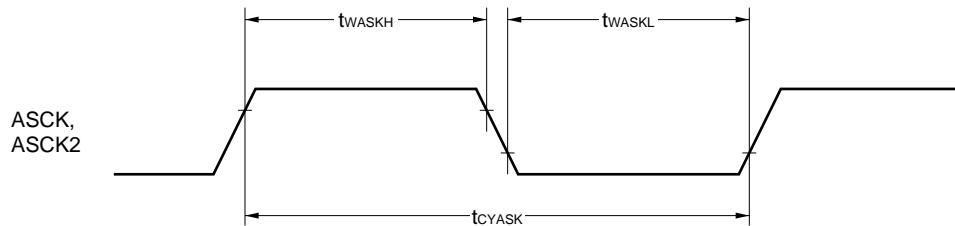
**SERIAL OPERATION (CSI, CSI3)**



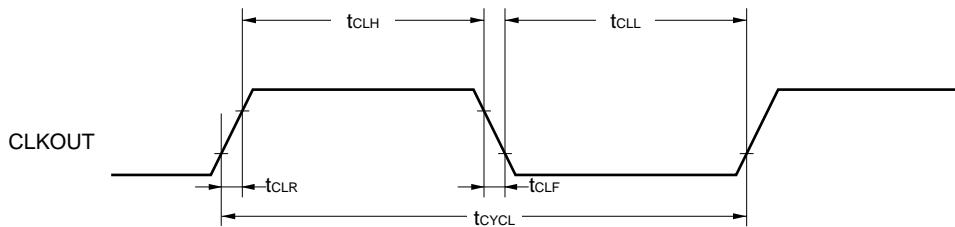
**SERIAL OPERATION (IOE1, IOE2)**



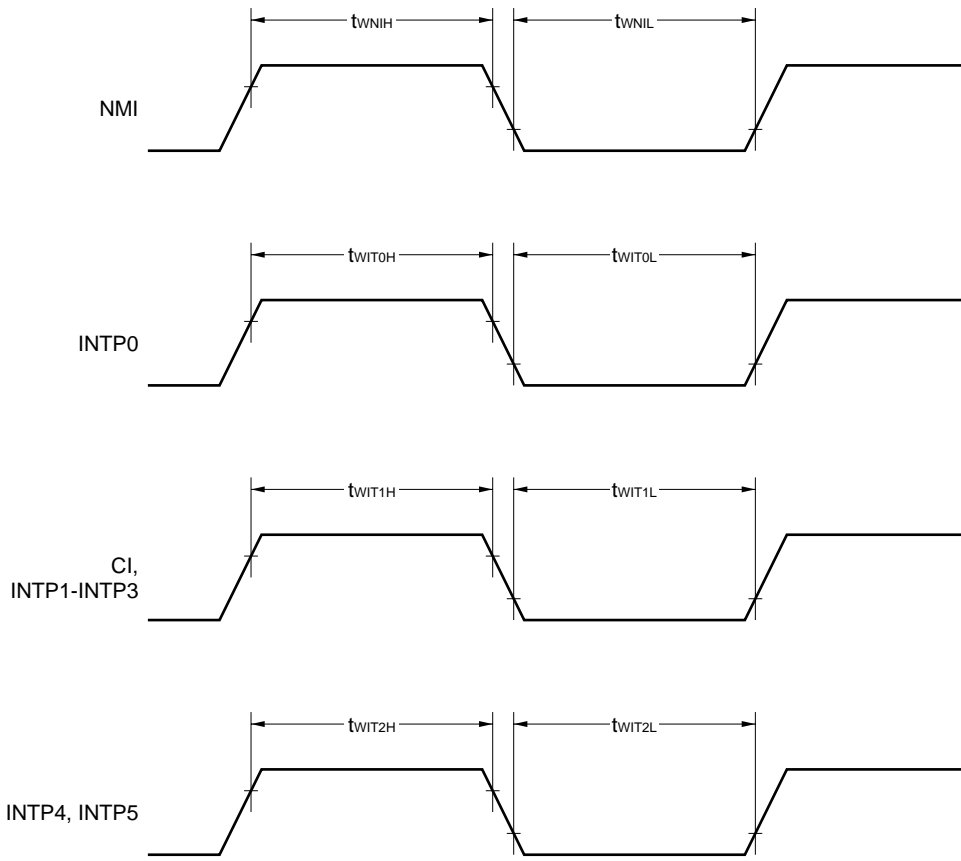
**SERIAL OPERATION (UART, UART2)**



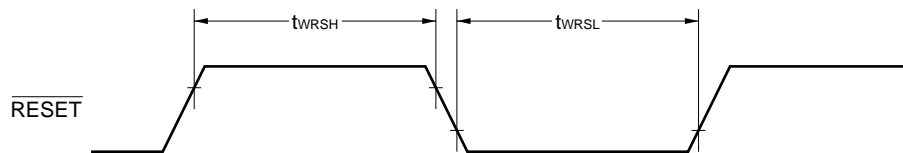
**CLOCK OUTPUT TIMING**



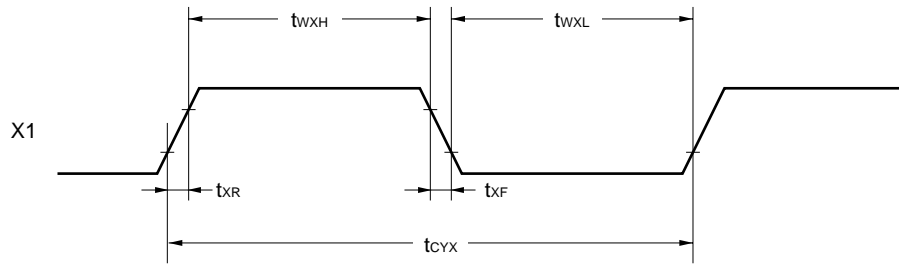
**INTERRUPT REQUEST INPUT TIMING**



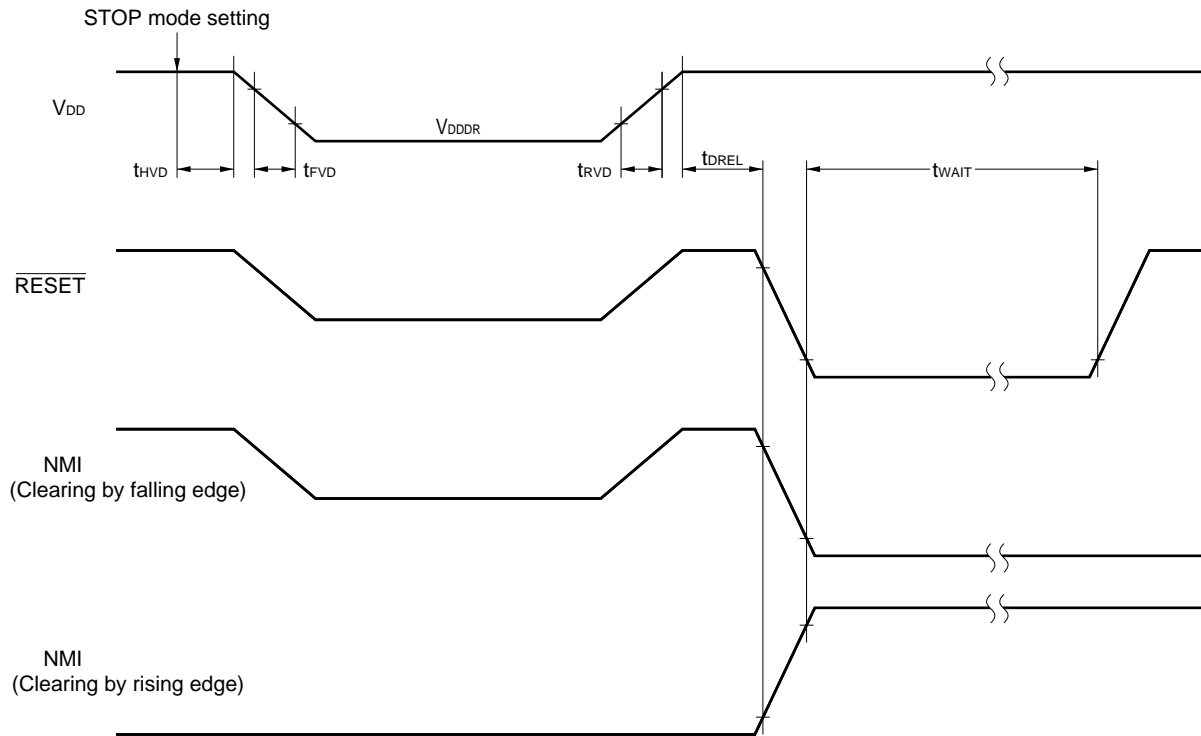
**RESET INPUT TIMING**



EXTERNAL CLOCK TIMING



DATA RETENTION CHARACTERISTICS



DC PROGRAMMING CHARACTERISTICS (T<sub>A</sub> = 25°C ±5°C, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Symbol <sup>Note 1</sup>	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V <sub>IH</sub>	V <sub>IH</sub>		2.2		V <sub>DDP</sub> + 0.3	V
Low-level input voltage	V <sub>IL</sub>	V <sub>IL</sub>		-0.3		+0.8	V
Input leakage current	I <sub>LIP</sub>	I <sub>LI</sub>	0 ≤ V <sub>I</sub> ≤ V <sub>DDP</sub> <sup>Note 2</sup>			±10	μA
High-level output voltage	V <sub>OH</sub>	V <sub>OH</sub>	I <sub>OH</sub> = -400 μA	2.4			V
Low-level output voltage	V <sub>OL</sub>	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA			0.45	V
Output leakage current	I <sub>LO</sub>	-	0 ≤ V <sub>O</sub> ≤ V <sub>DDP</sub> , $\overline{OE} = V_{IH}$			±10	μA
V <sub>DDP</sub> supply voltage	V <sub>DDP</sub>	V <sub>CC</sub>	Program memory write mode	6.25	6.5	6.75	V
			Program memory read mode	4.5	5.0	5.5	V
V <sub>PP</sub> supply voltage	V <sub>PP</sub>	V <sub>PP</sub>	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	V <sub>PP</sub> = V <sub>DDP</sub>			V
V <sub>DDP</sub> supply current	I <sub>DD</sub>	I <sub>DD</sub>	Program memory write mode		10	40	mA
			Program memory read mode		10	40	mA
V <sub>PP</sub> supply current	I <sub>PP</sub>	I <sub>PP</sub>	Program memory write mode		5	50	mA
			Program memory read mode		1.0	100	μA

- Notes**
1. Symbols for the corresponding μPD27C1001A
  2. The V<sub>DDP</sub> represents the V<sub>DD</sub> pin as viewed in the programming mode.

AC PROGRAMMING CHARACTERISTICS (T<sub>A</sub> = 25°C ±5°C, V<sub>SS</sub> = 0 V)

PROM Write Mode (Page Program Mode)

Parameter	Symbol <sup>Note 1</sup>	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time	t <sub>AS</sub>		2			μs
$\overline{CE}$ set time	t <sub>CES</sub>		2			μs
Input data setup time	t <sub>DS</sub>		2			μs
Address hold time	t <sub>AH</sub>		2			μs
	t <sub>AHL</sub>		2			μs
	t <sub>AHV</sub>		0			μs
Input data hold time	t <sub>DH</sub>		2			μs
Output data hold time	t <sub>DF</sub>		0		130	ns
V <sub>PP</sub> setup time	t <sub>VPS</sub>		2			μs
V <sub>DDP</sub> setup time	t <sub>VDS</sub> <sup>Note 2</sup>		2			μs
Initial program pulse width	t <sub>PW</sub>		0.095	0.1	0.105	ms
$\overline{OE}$ set time	t <sub>OES</sub>		2			μs
Valid data delay time from $\overline{OE}$	t <sub>OE</sub>			1	2	ns
$\overline{OE}$ pulse width in the data latch	t <sub>LW</sub>		1			μs
$\overline{PGM}$ setup time	t <sub>PGMS</sub>		2			μs
$\overline{CE}$ hold time	t <sub>CEH</sub>		2			μs
$\overline{OE}$ hold time	t <sub>OEH</sub>		2			μs

**Notes 1.** These symbols (except t<sub>VDS</sub>) correspond to those of the corresponding μPD27C1001A.

**2.** For μPD27C1001A, read t<sub>VDS</sub> as t<sub>VCS</sub>.

**PROM Write Mode (Byte Program Mode)**

Parameter	Symbol <sup>Note 1</sup>	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time	t <sub>AS</sub>		2			μs
$\overline{CE}$ set time	t <sub>CES</sub>		2			μs
Input data setup time	t <sub>DS</sub>		2			μs
Address hold time	t <sub>AH</sub>		2			μs
Input data hold time	t <sub>DH</sub>		2			μs
Output data hold time	t <sub>DF</sub>		0		130	ns
V <sub>PP</sub> setup time	t <sub>VPS</sub>		2			μs
V <sub>DDP</sub> setup time	t <sub>VDS</sub> <sup>Note 2</sup>		2			μs
Initial program pulse width	t <sub>PW</sub>		0.095	0.1	0.105	ms
$\overline{OE}$ set time	t <sub>OES</sub>		2			μs
Valid data delay time from $\overline{OE}$	t <sub>OE</sub>			1	2	ns

**Notes 1.** These symbols (except t<sub>VDS</sub>) correspond to those of the corresponding μPD27C1001A.

**2.** For μPD27C1001A, read t<sub>VDS</sub> as t<sub>VCS</sub>.

**PROM Read Mode**

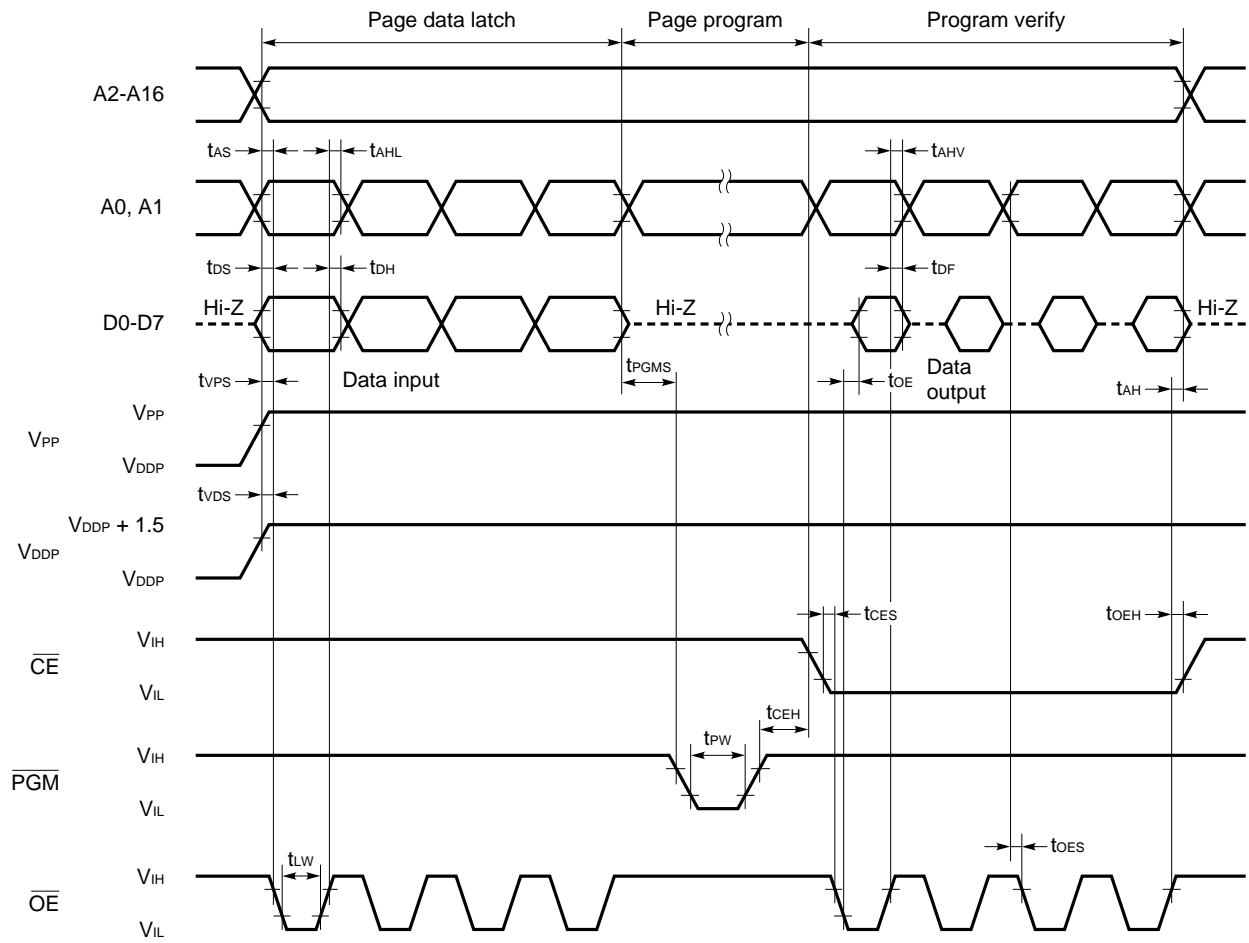
Parameter	Symbol <sup>Note 1</sup>	Conditions	MIN.	TYP.	MAX.	Unit
Data output time from address	t <sub>ACC</sub>	$\overline{CE} = \overline{OE} = V_{IL}$			200	ns
Delay from $\overline{CE} \downarrow$ to data output	t <sub>CE</sub>	$\overline{OE} = V_{IL}$		1	2	μs
Delay from $\overline{OE} \downarrow$ to data output	t <sub>OE</sub>	$\overline{CE} = V_{IL}$		1	2	μs
Data hold time to $\overline{OE} \uparrow$ or $\overline{CE} \uparrow$ <sup>Note 2</sup>	t <sub>DF</sub>	$\overline{CE} = V_{IL}$ or $\overline{OE} = V_{IL}$	0		60	ns
Data hold time to address	t <sub>OH</sub>	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

**Notes 1.** These symbols correspond to those of the corresponding μPD27C1001A.

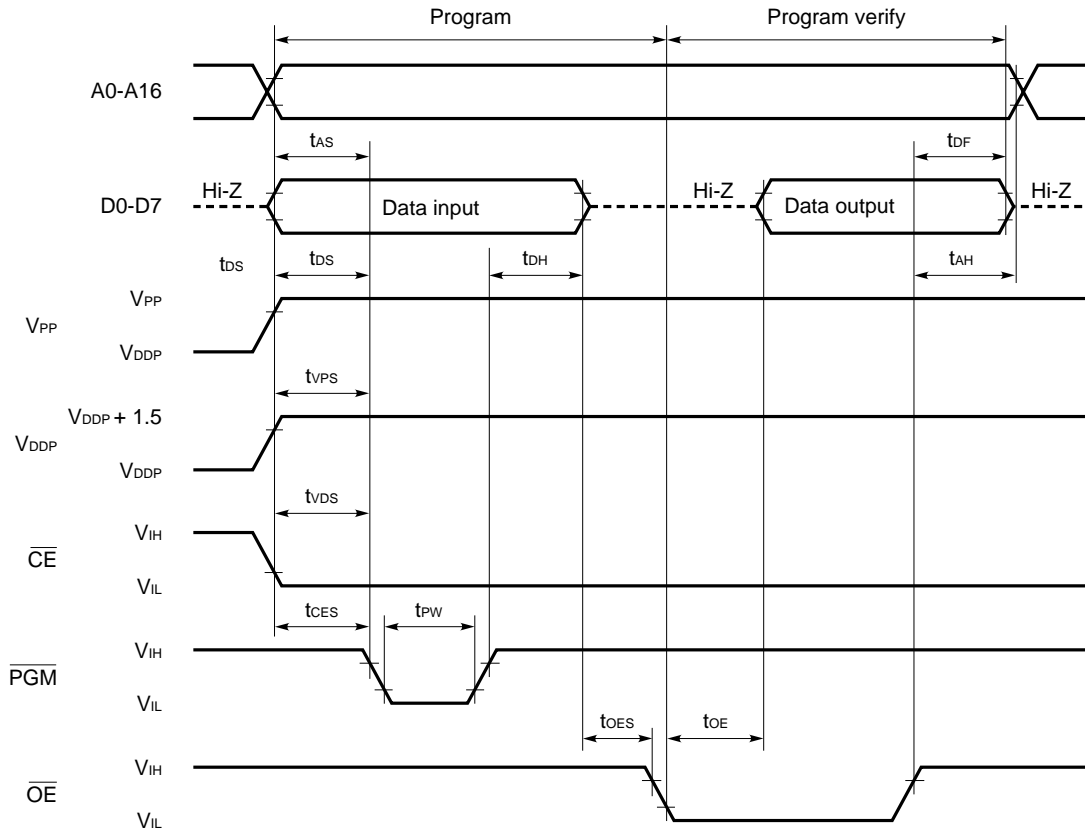
**2.** t<sub>DF</sub> is the time measured from when either  $\overline{OE}$  or  $\overline{CE}$  reaches V<sub>IH</sub>, whichever is faster.



PROM Write Mode Timing (Page Program Mode)

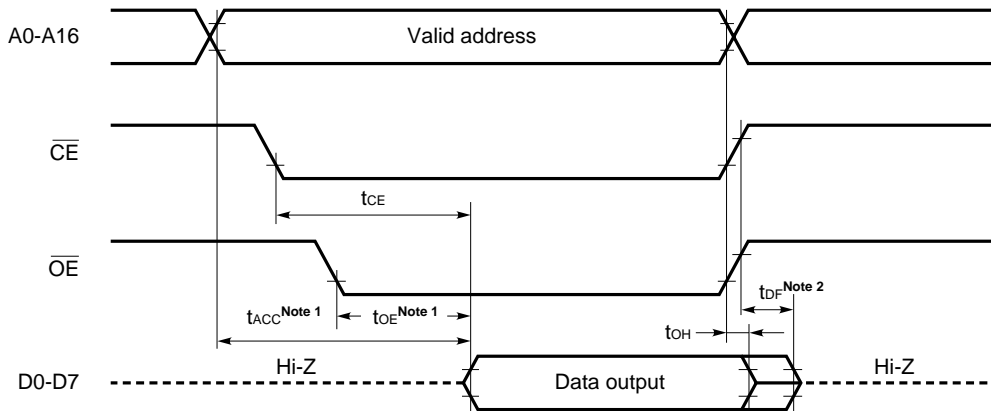


**PROM Write Mode Timing (Byte Program Mode)**



- Cautions**
1.  $V_{DDP}$  must be applied before  $V_{PP}$ , and must be cut after  $V_{PP}$ .
  2.  $V_{PP}$  including overshoot must not exceed 13.5 V.
  3. Plugging in or out the board with the  $V_{PP}$  pin supplied with 12.5 V may adversely affect its reliability.

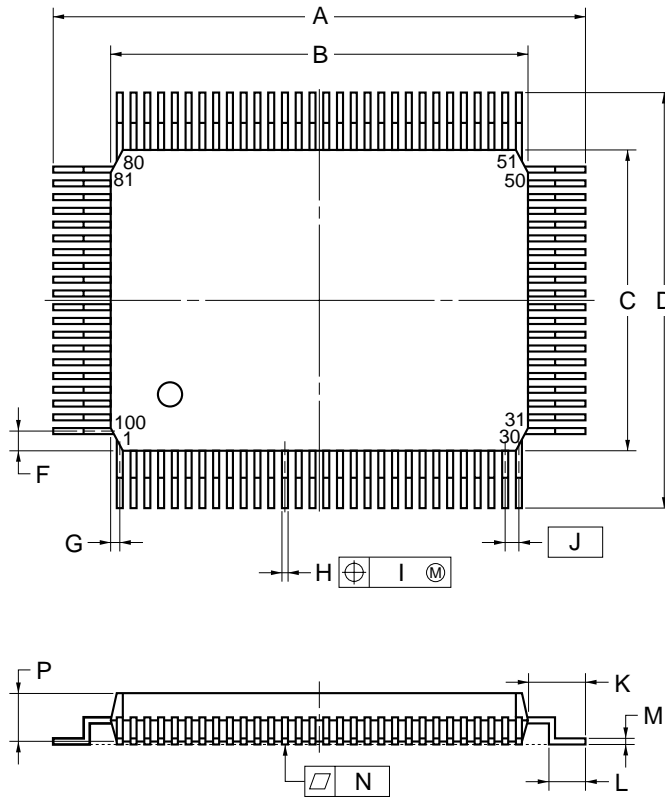
**PROM Read Mode Timing**



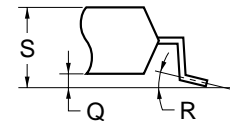
- Notes**
1. For reading within  $t_{ACC}$ , the delay of the  $\overline{OE}$  input from falling edge of  $\overline{CE}$  must be within  $t_{ACC}-t_{OE}$ .
  2.  $t_{DF}$  is the time measured from when either  $\overline{OE}$  or  $\overline{CE}$  reaches  $V_{IH}$ , whichever is faster.

9. PACKAGE DRAWING

100PIN PLASTIC QFP (14x20)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

**Remark** The shape and material of the ES version are the same as those of the corresponding mass-produced product.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	0.795 <sup>+0.009</sup> <sub>-0.008</sub>
C	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	0.012 <sup>+0.004</sup> <sub>-0.005</sub>
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	0.071 <sup>+0.008</sup> <sub>-0.009</sub>
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.10	0.004
P	2.7±0.1	0.106 <sup>+0.005</sup> <sub>-0.004</sub>
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P100GF-65-3BA1-3

**10. RECOMMENDED SOLDERING CONDITIONS**

The conditions listed below shall be met when soldering the μPD78P4908.

For details of the recommended soldering conditions, refer to our document **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

**Table 10-1. Soldering Conditions for Surface-Mount Devices**

**μPD78P4908GF-3BA: 100-pin plastic QFP (14 × 20 mm)**

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235°C Reflow time: 30 seconds or less (210°C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 7 days <b>Note</b> (20 hours of pre-baking is required at 125°C afterward)	IR35-207-2
VPS	Peak package's surface temperature: 215°C Reflow time: 40 seconds or less (200°C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 7 days <b>Note</b> (20 hours of pre-baking is required at 125°C afterward)	VP15-207-2
Wave soldering	Solder temperature: 260°C or less Flow time: 10 seconds or less Number of flow processes: 1 Preheating temperature: 120°C MAX. (measured on the package surface) Exposure limit: 7 days <b>Note</b> (20 hours of pre-baking is required at 125°C afterward)	WS60-207-1
Partial heating method	Terminal temperature: 300°C or less Heat time: 3 seconds or less (for one side of a device)	—

**Note** Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

**Caution** Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

**APPENDIX A DEVELOPMENT TOOLS**

The following development tools are available for system development using the μPD78P4908.

See also (5) **Notes on using development tools.**

**(1) Language processing software**

RA78K4	Assembler package for all 78K/IV series models
CC78K4	C compiler package for all 78K/IV series models
DF784908	Device file for μPD784908 subseries models
CC78K4-L	C compiler library source file for all 78K/IV series models

**(2) PROM write tools**

PG-1500	PROM programmer
PA-78P4908GF	Programmer adapter, connects to PG-1500
PG-1500 controller	Control program for PG-1500

**(3) Debugging tools**

- **When using the in-circuit emulator IE-78K4-NS**

	IE-78K4-NS	In-circuit emulator for all 78K/IV series models
	IE-70000-MC-PS-B	Power supply unit for IE-78K4-NS
★	IE-70000-98-IF-C	Interface adapter when the PC-9800 series computer (other than a notebook) is used as the host machine (C bus compatible)
★	IE-70000-CD-IF-A	PC card and interface cable when a notebook is used as the host machine (PCMCIA socket compatible)
★	IE-70000-PC-IF-C	Interface adapter when the IBM PC/AT™ compatible is used as the host machine (ISA compatible)
★	IE-7000-PCI-IF	Adapter when a computer with a PCI bus as the host machine
	IE-784908-NS-EM1 <sup>Note</sup>	Emulation board for evaluating μPD784908 subseries models
	NP-100GF <sup>Note</sup>	Emulation probe for 100-pin plastic QFP (GF-3BA type)
	EV-9200GF-100	Socket for mounting on target system board made for 100-pin plastic QFP (GF-3BA type). Used in LCC mode.
	ID78K4-NS	Integrated debugger for IE-78K4-NS
	SM78K4	System simulator for all 78K/IV series models
	DF784908	Device file for μPD784908 subseries models

**Note** Under development

• When using the in-circuit emulator IE-784000-R

	IE-784000-R	In-circuit emulator for all 78K/IV series models
★	IE-70000-98-IF-C	Interface adapter when the PC-9800 series computer (other than a notebook) is used as the host machine (C bus compatible)
★	IE-70000-PC-IF-C	Interface adapter when the IBM PC/AT compatible is used as the host machine (ISA bus compatible)
★	IE-7000-PCI-IF	Adapter when a computer with a PCI bus as the host machine
	IE-78000-R-SV3	Interface adapter and cable when the EWS is used as the host machine
	IE-784908-NS-EM1 IE-784908-R-EM1	Emulation board for evaluating μPD784908 subseries models
	IE-784000-R-EM	Emulation board for all 78K/IV series models
	IE-78K4-R-EX2	Conversion board for emulation probes required to use the IE-784908-NS-EM1 on the IE-784000-R. The board is not needed when the conventional product IE-784908-R-EM1 is used.
	EP-78064-GF-R	Emulation probe for 100-pin plastic QFP (GF-3BA type)
	EV-9200GF-100	Socket for mounting on target system board made for 100-pin plastic QFP (GF-3BA type)
	ID78K4	Integrated debugger for IE-784000-R
	SM78K4	System simulator for all 78K/IV series models
	DF784908	Device file for μPD784908 subseries models

(4) Real-time OS

RX78K/IV	Real-time OS for 78K/IV series models
MX78K4	OS for 78K/IV series models

**(5) Notes when using development tools**

- The ID78K4-NS, ID78K4, and SM78K4 can be used in combination with the DF784908.
- The CC78K4 and RX78K/IV can be used in combination with the RA78K4 and DF784908.
- The NP-100GF is a product from Naito Densai Machida Mfg. Co., Ltd. (044-822-3813). Consult the NEC sales representative for purchasing.
- The host machines and operating systems corresponding to each software are shown below.

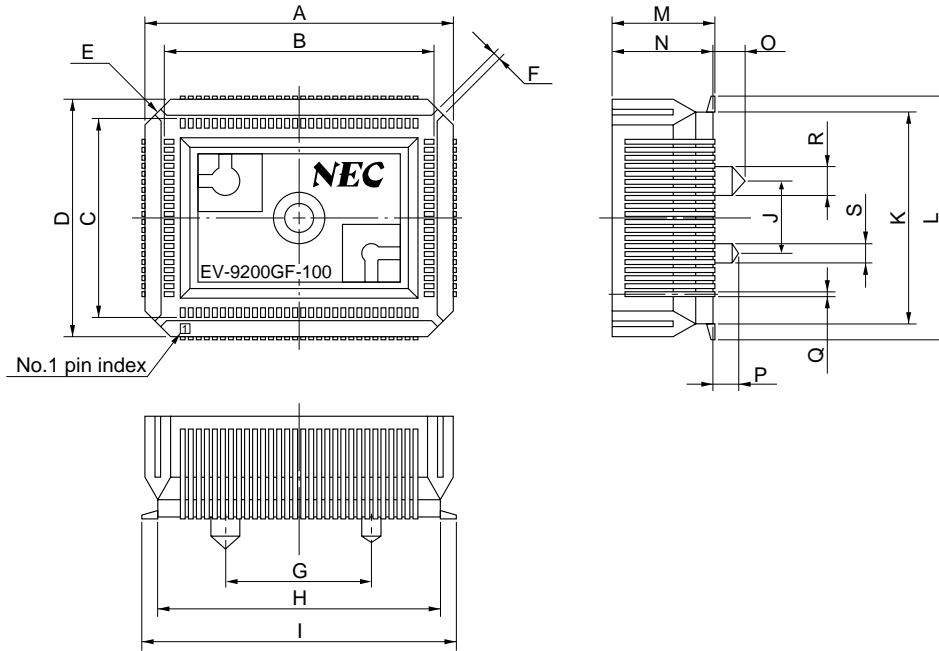
Host machine [OS]  Software	PC	EWS
	PC-9800 series [Windows™] IBM PC/AT compatibles [Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOST™, Solaris™] NEWST™ (RISC) [NEWS-OST™]
RA78K4	○ <b>Note</b>	○
CC78K4	○ <b>Note</b>	○
PG-1500 controller	○ <b>Note</b>	–
ID78K4-NS	○	–
ID78K4	○	○
SM78K4	○	–
RX78K/IV	○ <b>Note</b>	○
MX78K4	○ <b>Note</b>	○

**Note** Software under MS-DOS

APPENDIX B CONVERSION SOCKET (EV-9200GF-100) PACKAGE DRAWING

Connect the μPD78P4908GF-3BA (100-pin plastic QFP (14 × 20 mm)) to the circuit board in combination with the EV-9200GF-100.

Figure B-1. Package Drawings of EV-9200GF-100 (Reference)

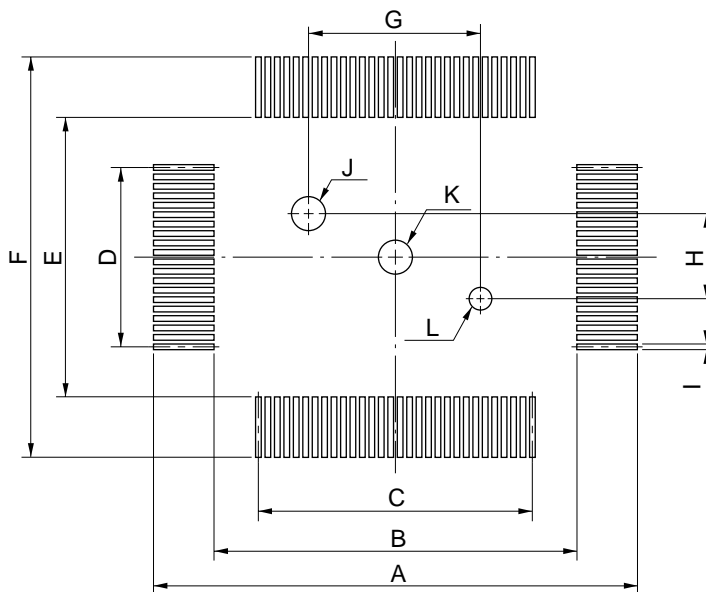


EV-9200GF-100-G0

ITEM	MILLIMETERS	INCHES
A	24.6	0.969
B	21	0.827
C	15	0.591
D	18.6	0.732
E	4-C 2	4-C 0.079
F	0.8	0.031
G	12.0	0.472
H	22.6	0.89
I	25.3	0.996
J	6.0	0.236
K	16.6	0.654
L	19.3	0.76
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059



Figure B-2. Recommended Pattern to Mount EV-9200GF-100 on a Substrate (Reference)



EV-9200GF-100-P1E

ITEM	MILLIMETERS	INCHES
A	26.3	1.035
B	21.6	0.85
C	$0.65 \pm 0.02 \times 29 = 18.85 \pm 0.05$	$0.026^{+0.001}_{-0.002} \times 1.142 = 0.742^{+0.002}_{-0.002}$
D	$0.65 \pm 0.02 \times 19 = 12.35 \pm 0.05$	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
E	15.6	0.614
F	20.3	0.799
G	$12 \pm 0.05$	$0.472^{+0.003}_{-0.002}$
H	$6 \pm 0.05$	$0.236^{+0.003}_{-0.002}$
I	$0.35 \pm 0.02$	$0.014^{+0.001}_{-0.001}$
J	$\phi 2.36 \pm 0.03$	$\phi 0.093^{+0.001}_{-0.002}$
K	$\phi 2.3$	$\phi 0.091$
L	$\phi 1.57 \pm 0.03$	$\phi 0.062^{+0.001}_{-0.002}$

**Caution** Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

**APPENDIX C RELATED DOCUMENTS**

**Documents Related to Devices**

Document name		Document No.	
		Japanese	English
μPD784907, 784908 Data Sheet		U11680J	U11680E
μPD78P4908 Data Sheet		U11681J	This document
μPD784908 Subseries User's Manual – Hardware		U11787J	U11787E
μPD784908 Subseries Special Function Registers		U11589J	—
78K/IV Series User's Manual – Instruction		U10905J	U10905E
78K/IV Series Instruction Table		U10594J	—
78K/IV Series Instruction Set		U10595J	—
78K/IV Series Application Note	Software Basic	U10095J	U10095E

**Documents Related to Development Tools (User's Manual)**

Document name		Document No.	
		Japanese	English
RA78K4 Assembler Package	Operation	U11334J	U11334E
	Language	U11162J	U11162E
RA78K Series Structured Assembler Preprocessor		U11743J	U11743E
CC78K4 C Compiler	Operation	U11572J	U11572E
	Language	U11571J	U11571E
PG-1500 PROM Programmer		U11940J	U11940E
PG-1500 Controller PC-9800 Series (MS-DOS™) Base		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS™) Base		EEU-5008	U10540E
★	IE-78K4-NS	U13356J	U13356E
	IE-784000-R	U12903J	U12903E
	IE-784908-R-EM1	U11876J	—
★	IE-784908-NS-EM1	U13743J	On preparation
EP-78064		EEU-934	EEU-1469
SM78K4 System Simulator Windows Base	Reference	U10093J	U10093E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
ID78K4-NS Integrated Debugger PC Base	Reference	U12796J	U12796E
ID78K4 Integrated Debugger Windows Base	Reference	U10440J	U10440E
ID78K4 Integrated Debugger HP-UX, SunOS, NEWS-OS Base	Reference	U11960J	U11960E

**Caution** The above documents may be revised without notice. Use the latest versions when you design application systems.

**Documents Related to Software to Be Incorporated into the Product (User's Manual)**

Document name		Document No.	
		Japanese	English
78K/IV Series Real-Time OS	Fundamental	U10603J	U10603E
	Installation	U10604J	U10604E
	Debugger	U10364J	—
OS for 78K/IV Series MX78K4	Fundamental	U11779J	—

**Other Documents**

★

Document name	Document No.	
	Japanese	English
NEC IC Package Manual (CD-ROM)	—	C13388E
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Quality Assurance for Semiconductor Devices	—	MEI-1202
Guide for Products Related to Microcomputer: Other Companies	U11416J	—

**Caution** The above documents may be revised without notice. Use the latest versions when you design application systems.

[MEMO]

[MEMO]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

## Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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### **NEC Electronics Inc. (U.S.)**

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800-366-9782  
Fax: 408-588-6130  
800-729-9288

### **NEC Electronics (Germany) GmbH**

Duesseldorf, Germany  
Tel: 0211-65 03 02  
Fax: 0211-65 03 490

### **NEC Electronics (UK) Ltd.**

Milton Keynes, UK  
Tel: 01908-691-133  
Fax: 01908-670-290

### **NEC Electronics Italiana s.r.l.**

Milano, Italy  
Tel: 02-66 75 41  
Fax: 02-66 75 42 99

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Fax: 91-504-2860

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Taeby, Sweden  
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Fax: 08-63 80 388

### **NEC Electronics Hong Kong Ltd.**

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Fax: 2886-9022/9044

### **NEC Electronics Hong Kong Ltd.**

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Fax: 02-528-4411

### **NEC Electronics Singapore Pte. Ltd.**

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Tel: 65-253-8311  
Fax: 65-250-3583

### **NEC Electronics Taiwan Ltd.**

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Fax: 02-2719-5951

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NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

**Standard:** Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

**Special:** Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

**Specific:** Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.